100V 60A N-Channel Enhancement Mode Power MOSFET

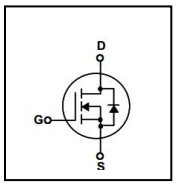
General Description

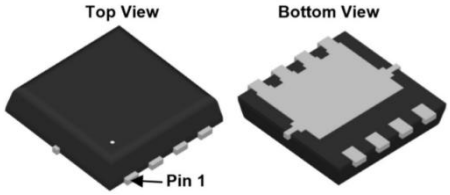
BXS095N10C is fabricated using advanced trench technology. The resulting device has extremely low on resistance, making it especially suitable for applications which require superior power density and outstanding efficiency.

FEATURES

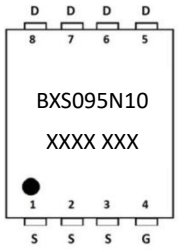
- RDSON≤9.5mΩ @Vgs=10V, Id=30A
- Excellent RDS(ON) and Low Gate Charge
- 100% avalanche tested
- Lead free product is acquired

SYMBOL





PDFN5X6-8L



Marking and pin Assignment

ASSEMBLY MESSAGE

Product Name	Marking	Package	Reel (PCS)	Per Carton (PCS)
BXS095N10C	BXS095N10	PDFN5*6-8L	2500	25000

ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Parameter		Symbol	Rating	Unit
			PDFN5*6-8L	
Drain-Source Voltage		V_{DSS}	100	V
Drain Current	Continuous (T_C = 25°C)	I_D	60	A
	Continuous (T_C = 100°C)		38	A
Drain Current	Pulsed (Note1)	I_{DM}	240	A
Gate-Source Voltage		V_{GSS}	±20	V
Avalanche Energy	Single Pulse (Note2)	E_{AS}	90	mJ
Power Dissipation (Note 2)	T_C =25°C	P_D	62.5	W
Maximum Junction Temperature		T_J	150	°C
Storage Temperature Range		T_{STG}	-55 to 150	°C

Note： 1. Repetitive Rating: Pulse width limited by maximum junction temperature

2. L=0.5mH, I_{AS}=19A, V_{DD}=50V, RG=25 Ω, Starting TJ = 25°C

THERMAL CHARACTERISTICS

Parameter	Symbol	Max.	Unit
		PDFN5*6-8L	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2	°C / W

ELECTRICAL CHARACTERISTICS（T_J=25℃,unless otherwise Noted）

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	VGS=0V, ID=250μA	100			V
Zero Gate Voltage Drain Current	I_{DSS}	VDS=100V, VGS=0V			1	uA
Gate-Body Leakage Current, Forward	I_{GSS}	VGS=20V			100	nA
Gate-Body Leakage Current, Reverse		VGS=-20V			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	VDS=VGS, ID=250μA	1.2	1.8	2.6	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	VGS=10V, ID=30A		8.2	9.5	mΩ
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	VDS=50V, VGS=0V, f=1.0MHz		2122		pF
Output Capacitance	C_{OSS}			618		pF
Reverse Transfer Capacitance	C_{RSS}			25		pF
SWITCHING PARAMETERS						
Turn-ON Delay Time	$t_{D(ON)}$	VDD=50V, ID=30A, VGS = 10V, RG=3Ω		17		ns
Turn-ON Rise Time	t_R			4		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			32		ns
Turn-OFF Fall-Time	t_F			8		ns
Total Gate Charge(Note4)	Q_G	VDS =50V, VGS =10V, ID =30A		41.8		nC
Gate Source Charge	Q_{GS}			9		nC
Gate Drain Charge	Q_{GD}			10		nC
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Drain-Source Diode Forward Voltage	V_{SD}	IS=30A, VGS=0V		0.88	1.0	V
Diode Continuous Forward Current	I_S				60	A
Reverse Recovery Time	t_{RR}	VGS = 0 V, ISD = 30A di/dt=100 A/μs		50.5		ns
Reverse Recovery Charge	Q_{RR}			71.5		nC

Note： 3. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%

4. Essentially independent of operating temperature

TYPICAL CHARACTERISTICS

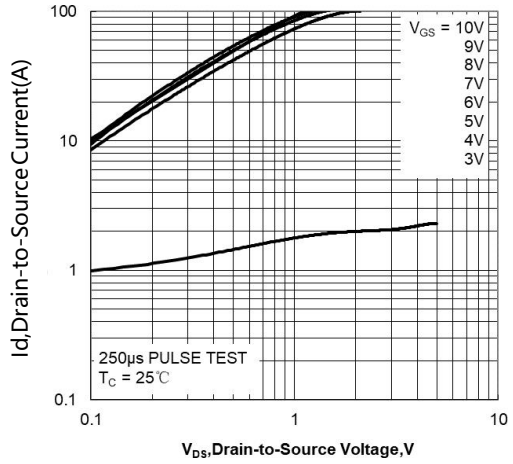


Figure1. Typical Output Characteristics

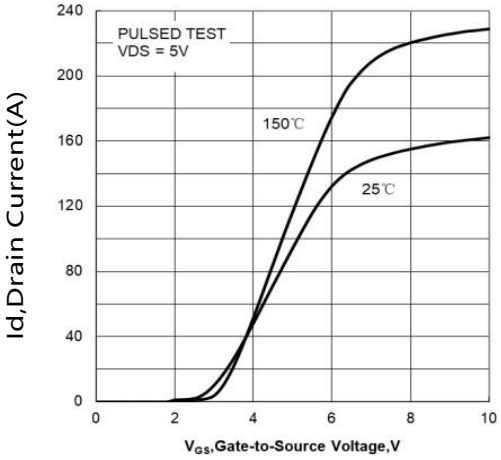


Figure2. Typical Transfer Characteristics

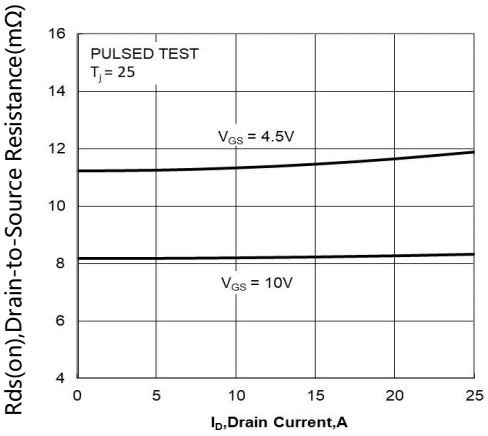


Figure3. On-Resistance versus Drain Current

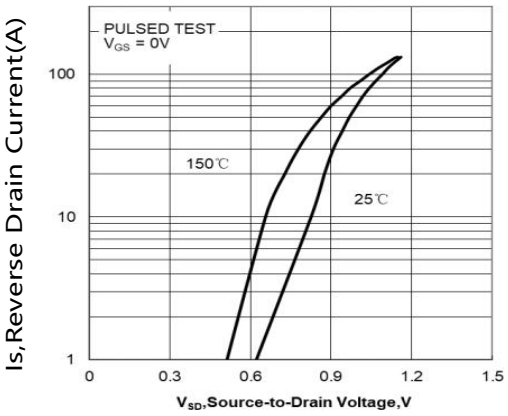


Figure4. Diode forward voltage versus Current

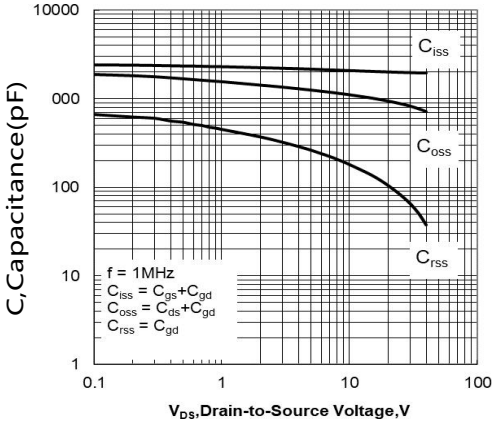


Figure5. Typical Capacitance versus V_{DS}

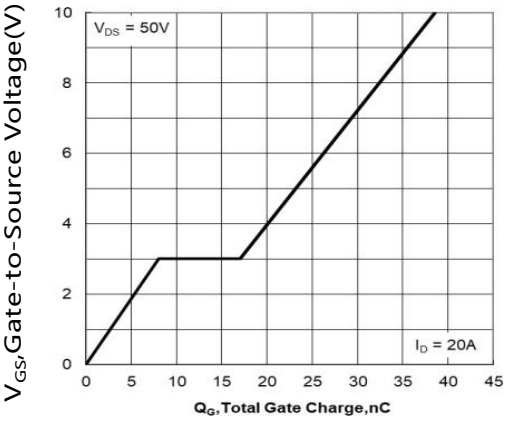


Figure6. Typical Gate Charge versus V_{GS}

TYPICAL CHARACTERISTICS(Cont.)

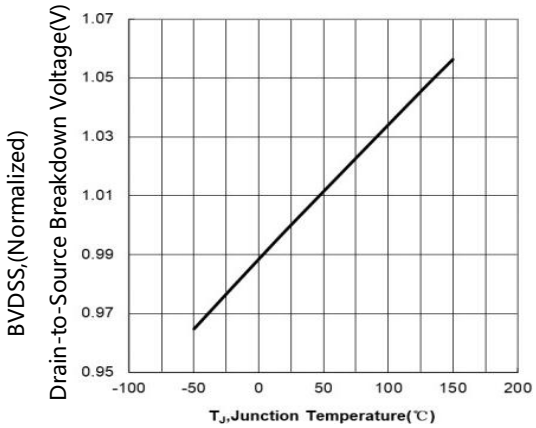


Figure7. BV_{DSS} Variation with Temperature

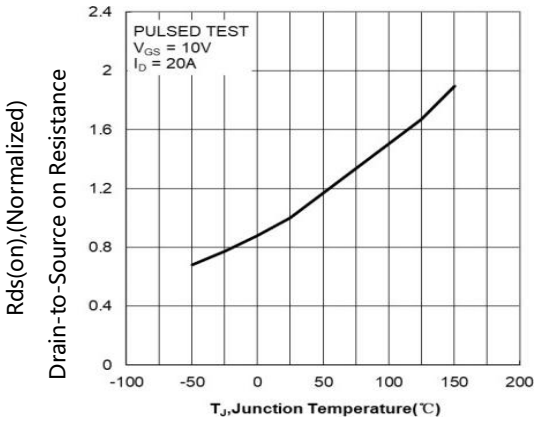


Figure8. On-Resistance Variation with Temperature

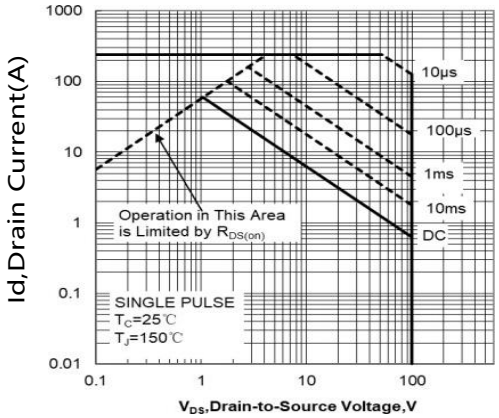


Figure9. Maximum Safe Operating Area

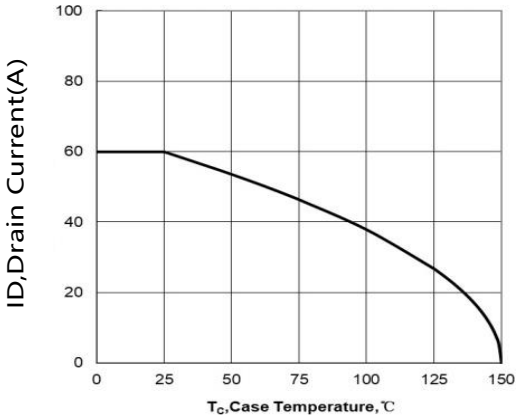
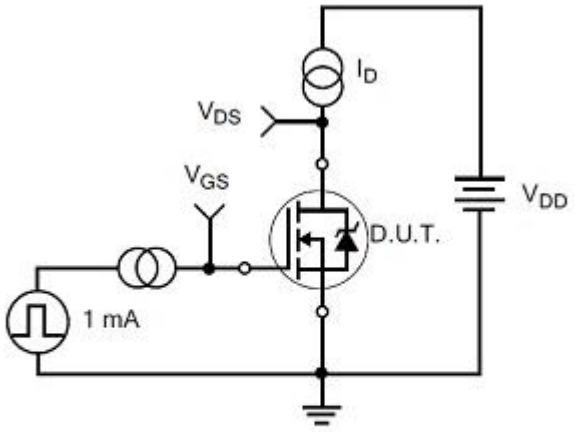
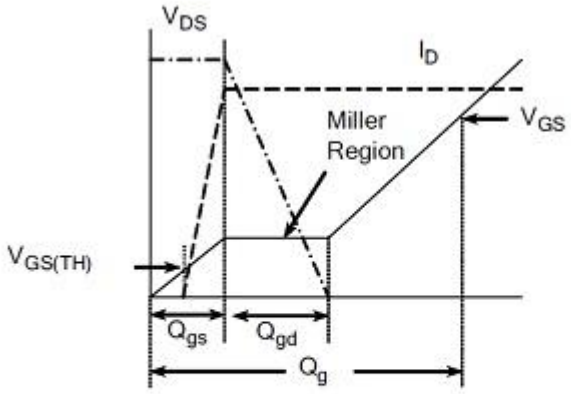


Figure10. Maximum Continuous Drain Current versus Case Temperature

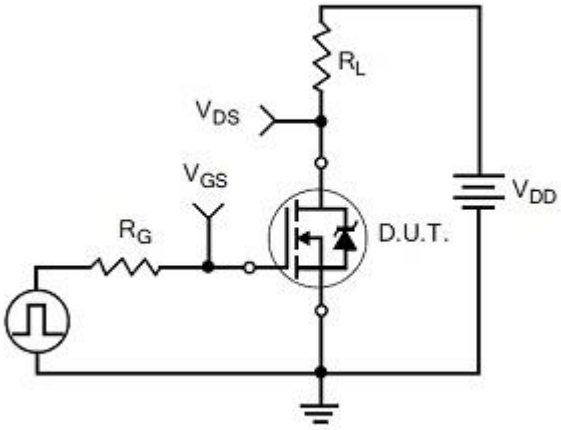
TEST CIRCUITS AND WAVEFORMS



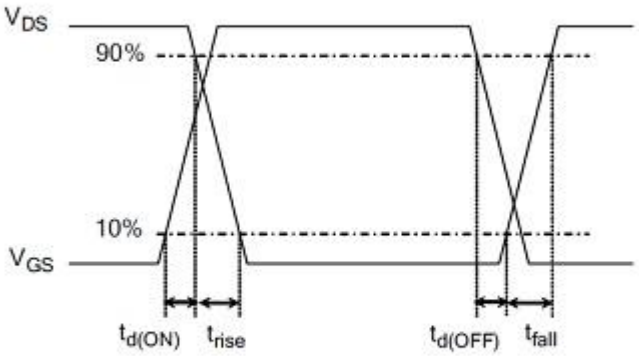
Gate Charge Test Circuit



Gate Charge Waveform

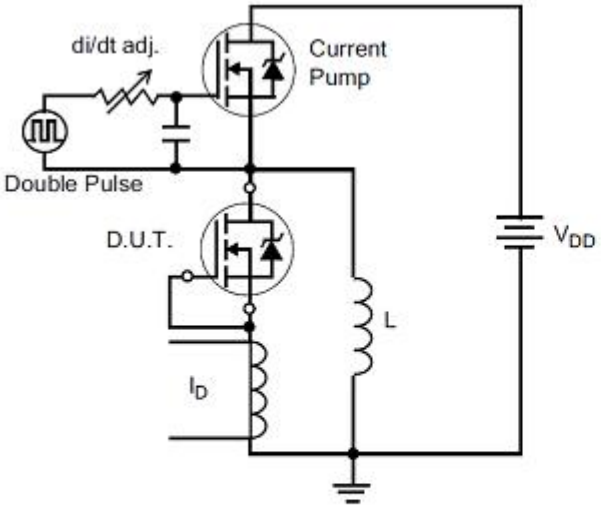


Resistive Switching Test Circuit

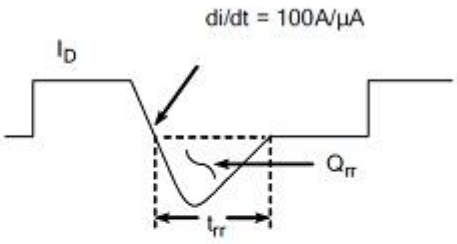


Resistive Switching Waveforms

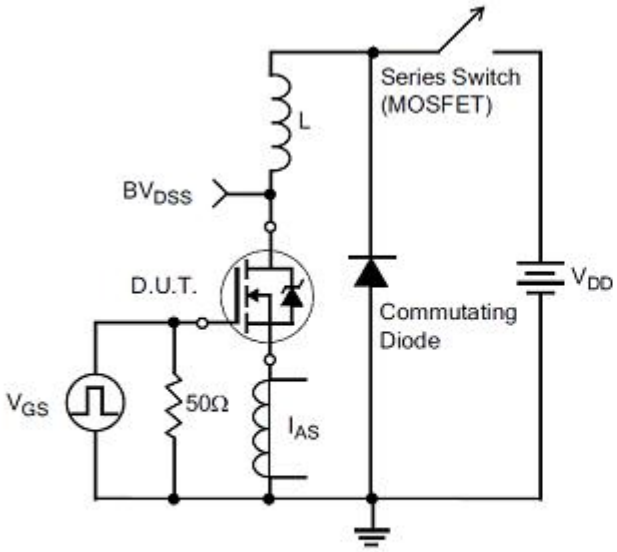
TEST CIRCUITS AND WAVEFORMS(Cont.)



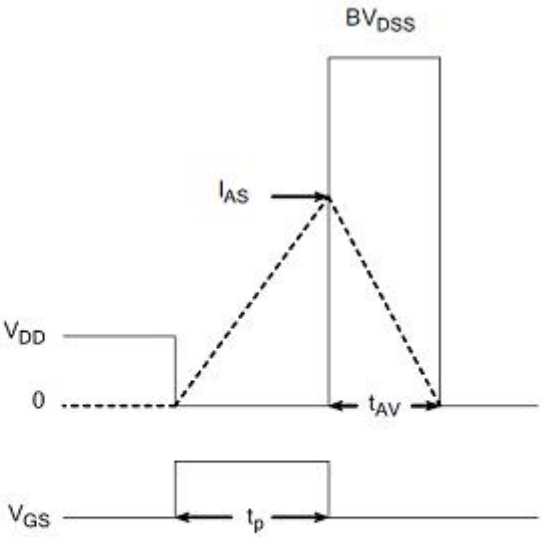
Diode Reverse Recovery Test Circuit



Diode Reverse Recovery Waveform



Unclamped Inductive Switching Test Circuit



$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

Unclamped Inductive Switching Waveforms

Revision history

Document revision history

Date	Revision	Changes
14-Sep-2021	1.0	First release
9-Oct-2021	1.1	Update layout format

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