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Xu

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(54) **SYSTEM FOR WAFER-LEVEL PHOSPHOR DEPOSITION**

(71) Applicant: **Bridgelux, Inc.**, Livermore, CA (US)

(72) Inventor: **Tao Xu**, Fremont, CA (US)

(73) Assignee: **Bridgelux, Inc.**, Livermore, CA (US)

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This patent is subject to a terminal disclaimer.

(21) Appl. No.: **14/479,031**

(22) Filed: **Sep. 5, 2014**

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Related U.S. Application Data

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(51) **Int. Cl.**

H01L 27/15	(2006.01)
H01L 33/50	(2010.01)
H01L 21/78	(2006.01)
H01L 21/66	(2006.01)
H01L 33/00	(2010.01)

(52) **U.S. Cl.**

CPC ***H01L 27/153*** (2013.01); ***H01L 21/78*** (2013.01); ***H01L 22/10*** (2013.01); ***H01L 33/005*** (2013.01); ***H01L 33/508*** (2013.01); *H01L 2933/0041* (2013.01); *H01L 2933/0058* (2013.01)

(58) **Field of Classification Search**

CPC H01L 27/153; H01L 21/78; H01L 22/10; H01L 33/005; H01L 33/508

USPC 257/79–93, 98; 438/22–26, 28, 29, 438/33–35, 46, 458, 460, 464

See application file for complete search history.

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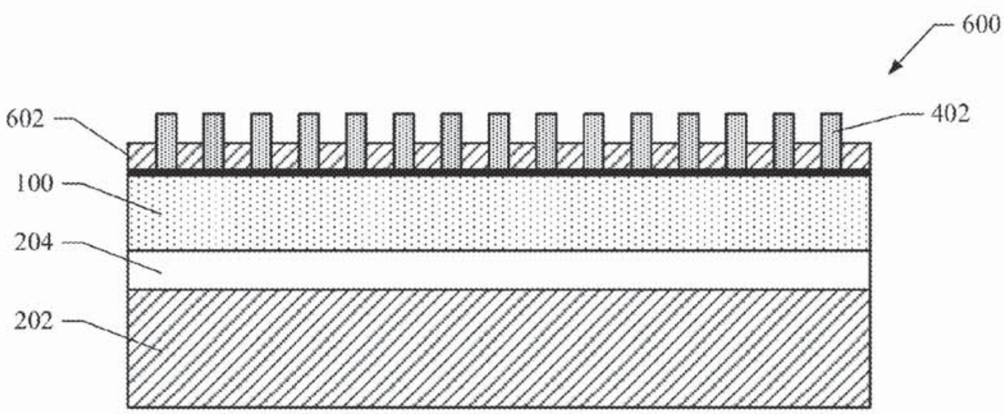
Primary Examiner — Ori Nadav

(74) *Attorney, Agent, or Firm* — James M. Wu; JW Law Group

(57) **ABSTRACT**

System for wafer-level phosphor deposition. A method for phosphor deposition on a semiconductor wafer that has a plurality of LED dies includes the operations of covering the semiconductor wafer with a selected thickness of photo resist material, removing portions of the photo resist material to expose portions of the semiconductor wafer so that electrical contacts associated with the plurality of LED dies remain unexposed, and depositing phosphor on the exposed portions of the semiconductor wafer.

19 Claims, 8 Drawing Sheets



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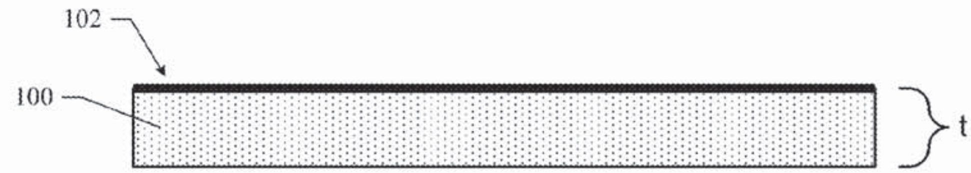


FIG. 1

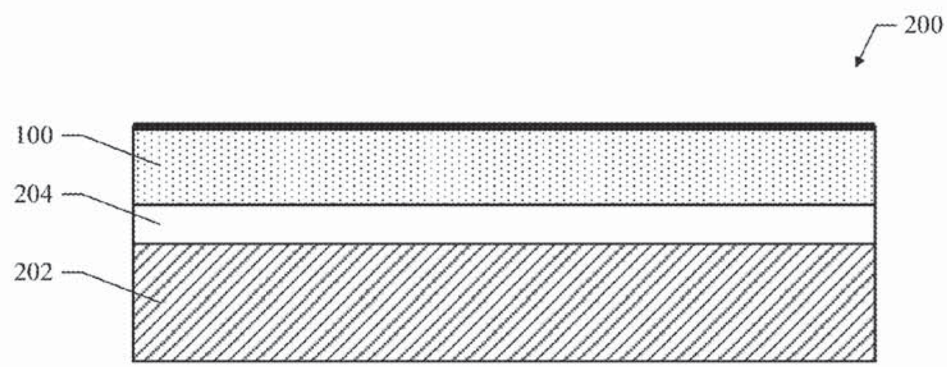


FIG. 2

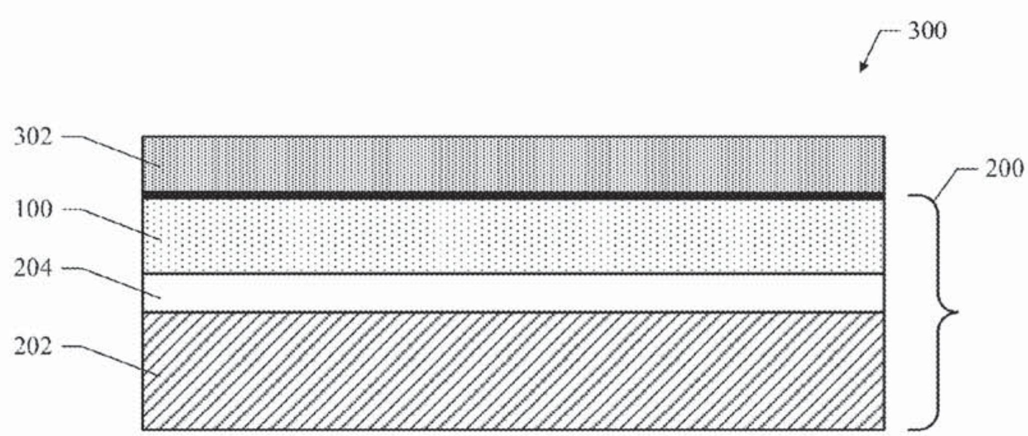


FIG. 3

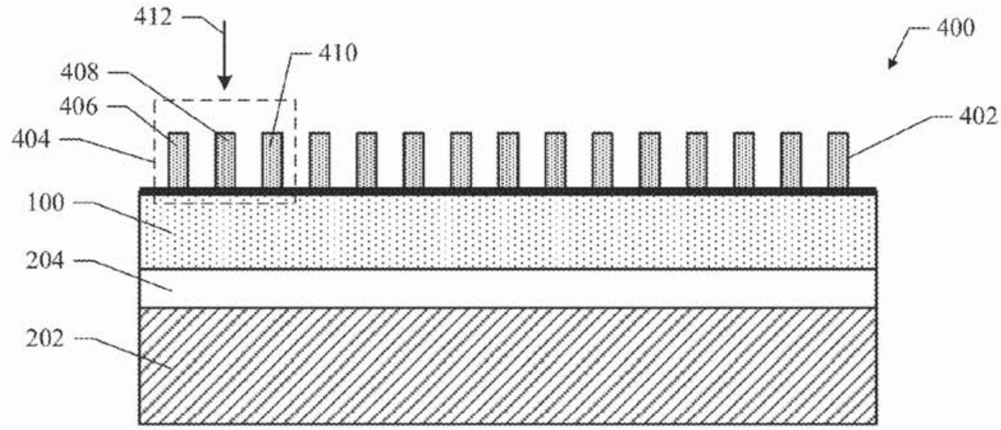


FIG. 4

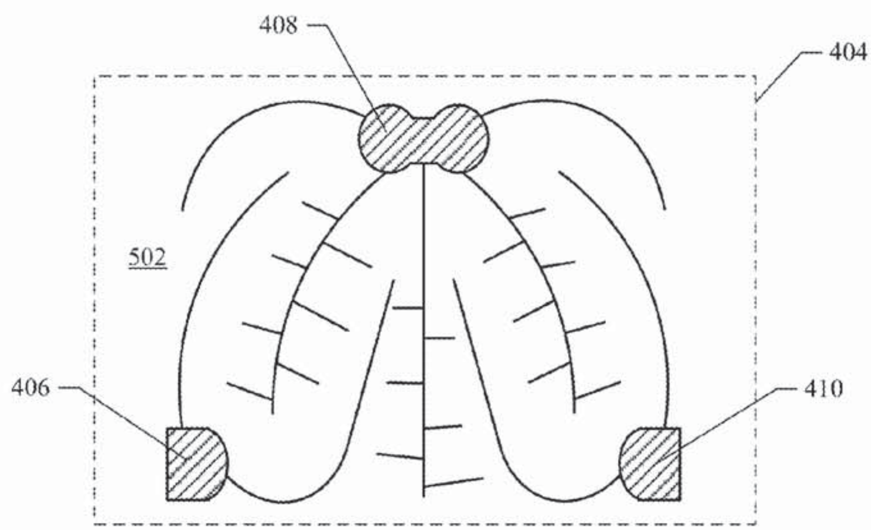


FIG. 5

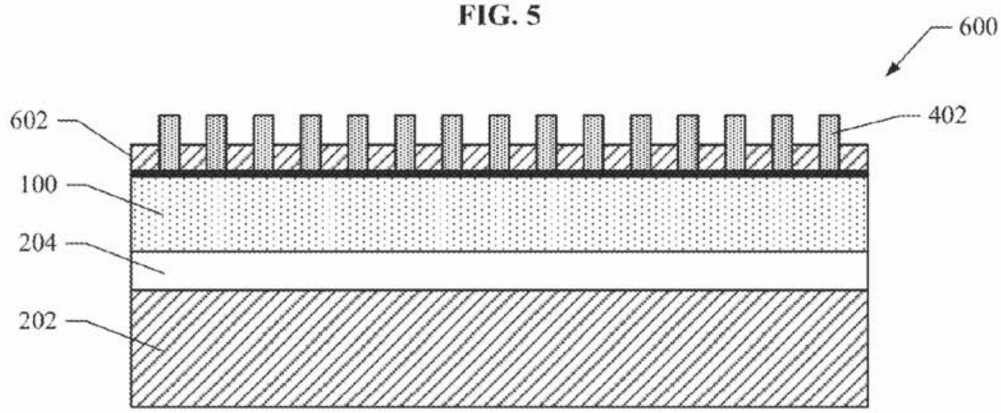


FIG. 6

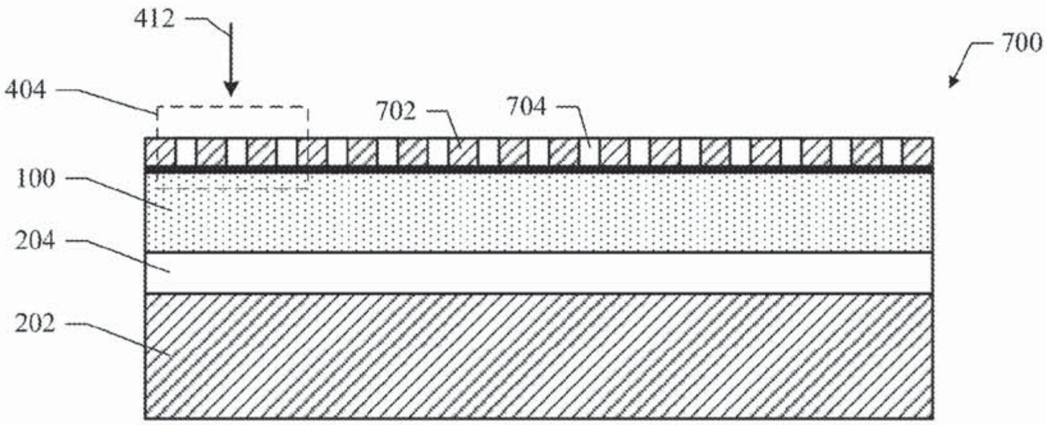


FIG. 7

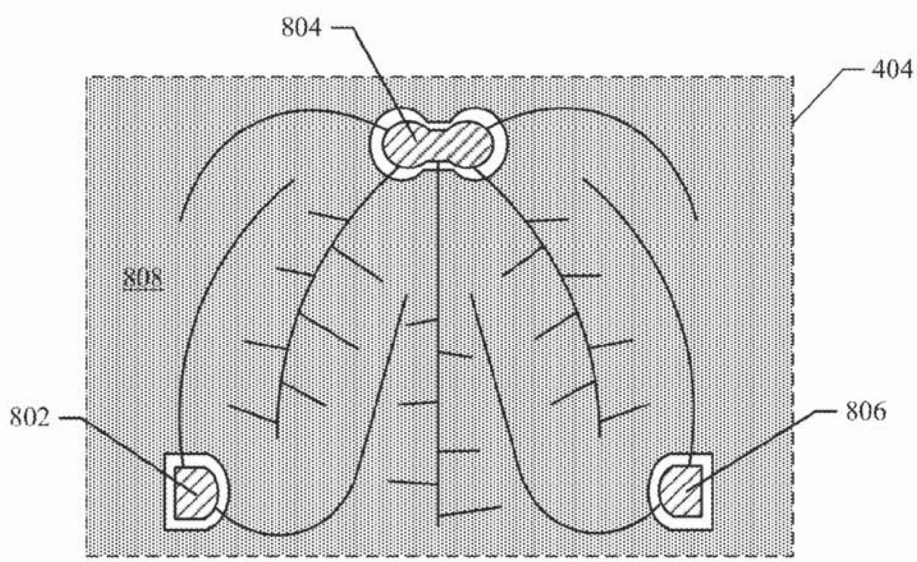


FIG. 8

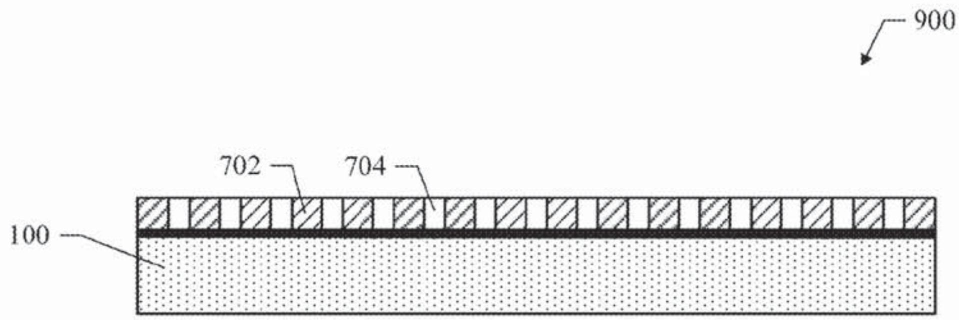


FIG. 9

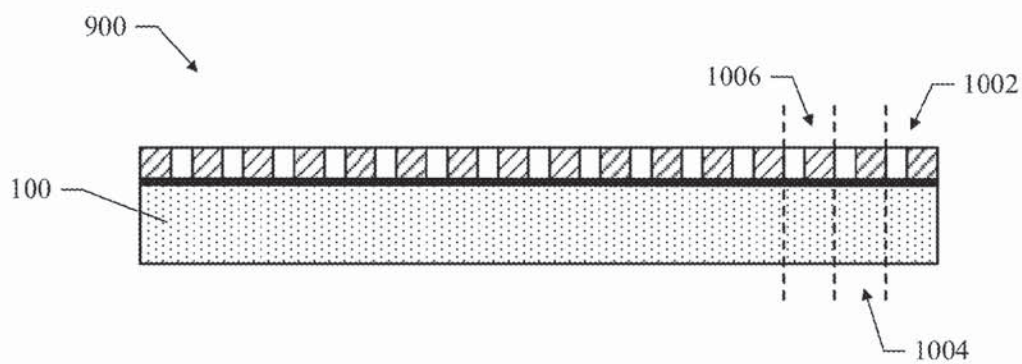


FIG. 10

1100

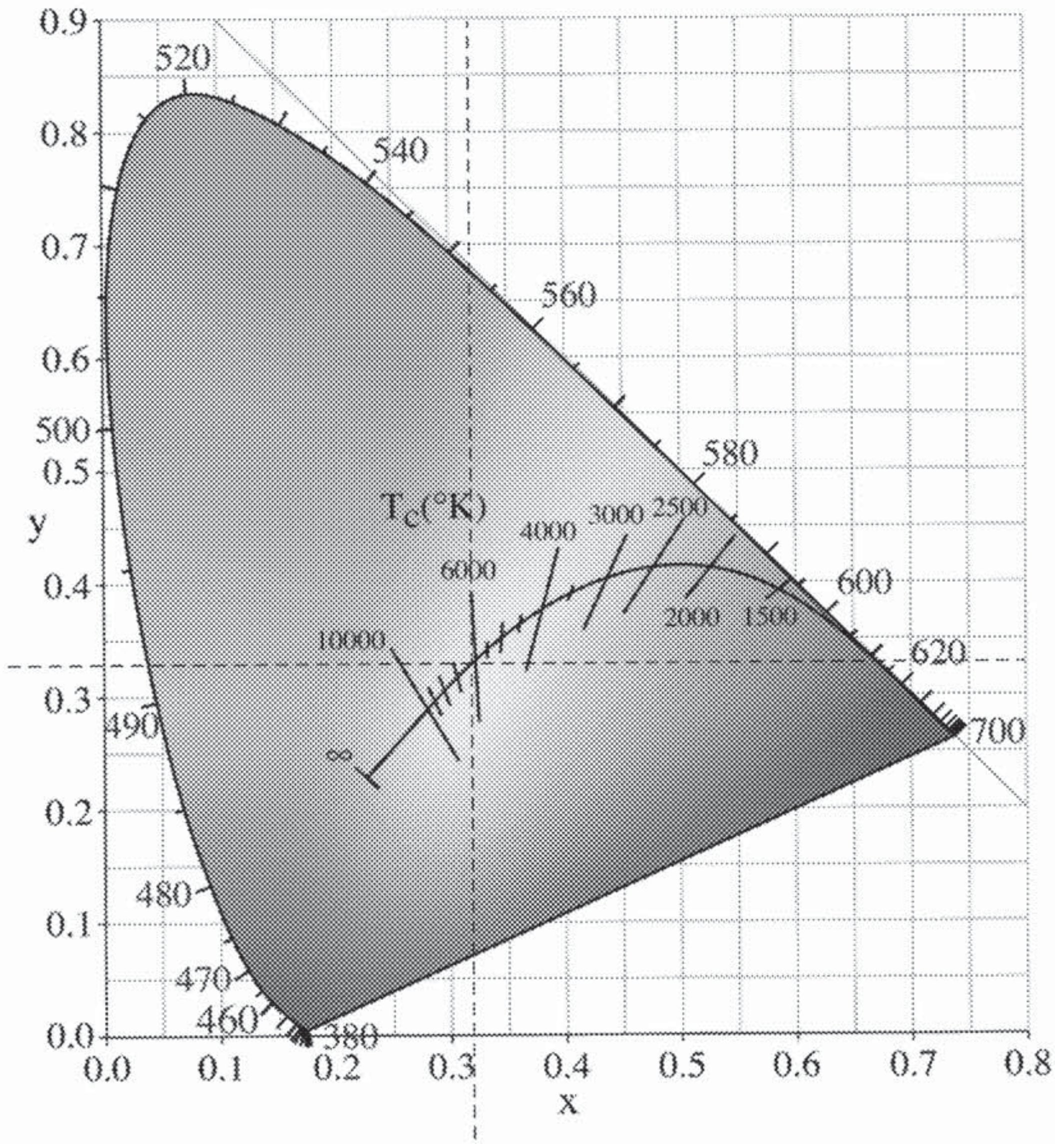
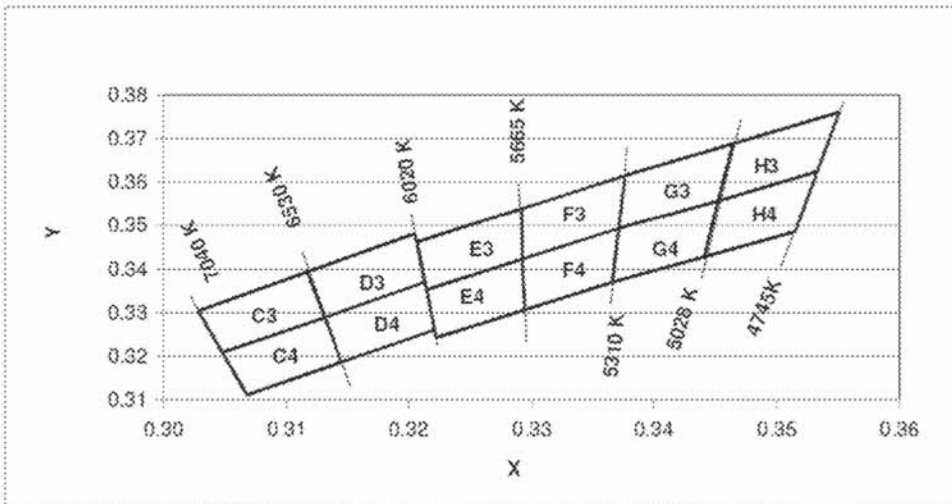

0.9
0.8
0.7
0.6
500
0.5
y
0.4
0.3
490
0.2
480
0.1
470
460
0.0
380
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
x
520
540
560
580
600
620
700
T_C(°K)
4000
3000
2500
6000
10000
2000
1500
∞

FIG. 11

1200



1202

Bin Code	X	Y	ANSI CCT (K)
C3	0.3048	0.3209	6500
	0.3131	0.3290	
	0.3117	0.3393	
	0.3028	0.3304	
C4	0.3068	0.3113	6500
	0.3145	0.3187	
	0.3131	0.3290	
	0.3048	0.3209	
D3	0.3131	0.3290	6500
	0.3213	0.3371	
	0.3205	0.3481	
	0.3117	0.3393	
D4	0.3145	0.3187	6500
	0.3221	0.3261	
	0.3213	0.3371	
	0.3131	0.3290	

Bin Code	X	Y	ANSI CCT (K)
E3	0.3215	0.3353	5700
	0.3293	0.3423	
	0.3292	0.3539	
	0.3207	0.3462	
E4	0.3222	0.3243	5700
	0.3294	0.3306	
	0.3293	0.3423	
	0.3215	0.3353	
F3	0.3292	0.3539	5700
	0.3293	0.3423	
	0.3371	0.3493	
	0.3376	0.3616	
F4	0.3294	0.3306	5700
	0.3366	0.3369	
	0.3371	0.3493	
	0.3293	0.3423	

Bin Code	X	Y	ANSI CCT (K)
G3	0.3376	0.3616	5000
	0.3464	0.3688	
	0.3452	0.3558	
	0.3371	0.3493	
G4	0.3371	0.3493	5000
	0.3452	0.3558	
	0.3441	0.3428	
	0.3366	0.3369	
H3	0.3464	0.3688	5000
	0.3551	0.3760	
	0.3533	0.3624	
	0.3452	0.3558	
H4	0.3452	0.3558	5000
	0.3533	0.3624	
	0.3515	0.3487	
	0.3441	0.3428	

1204

FIG. 12

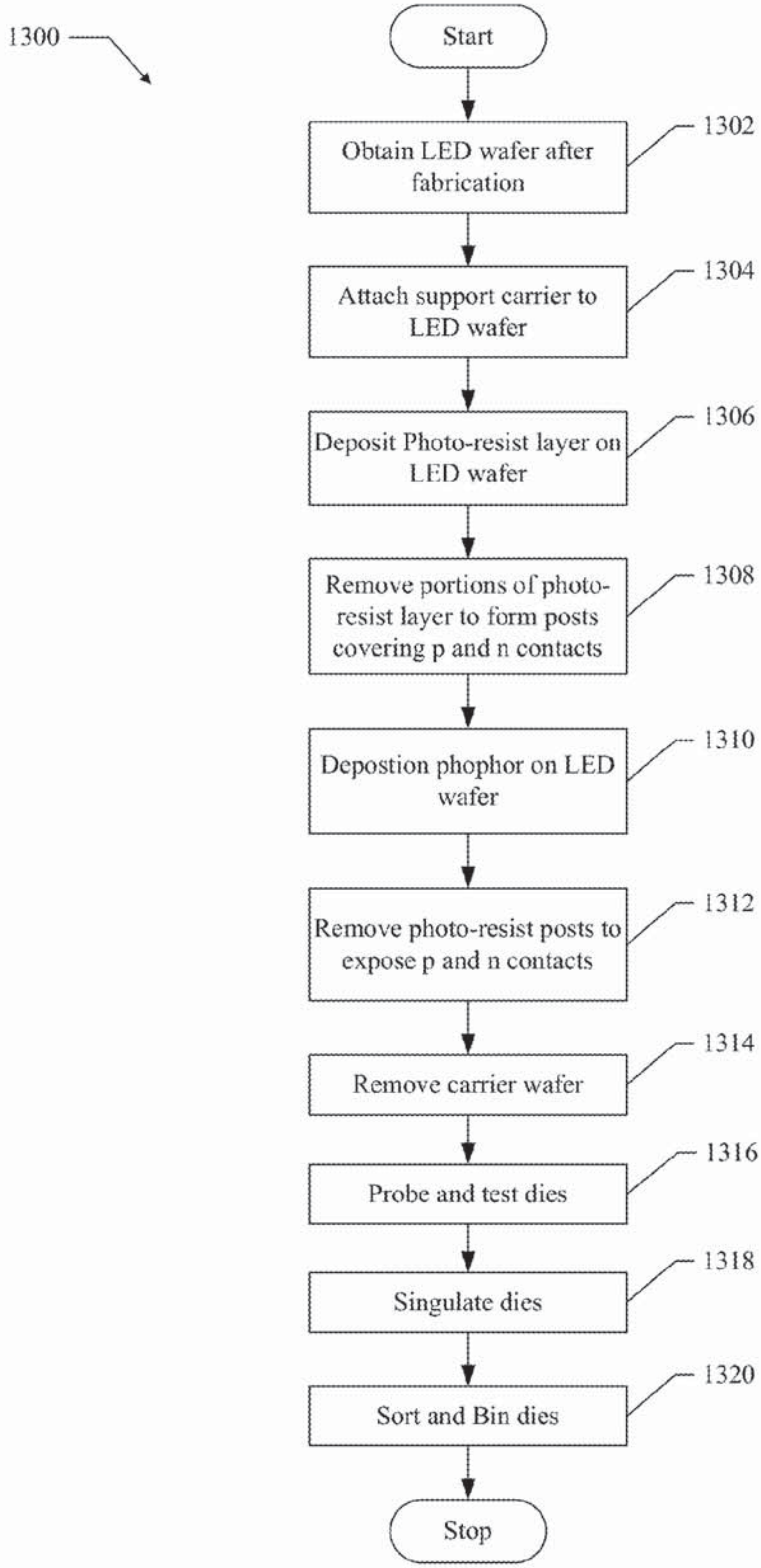

1300
Start
Obtain LED wafer after fabrication
1302
Attach support carrier to LED wafer
1304
Deposit Photo-resist layer on LED wafer
1306
Remove portions of photo-resist layer to form posts covering p and n contacts
1308
Depostion phophor on LED wafer
1310
Remove photo-resist posts to expose p and n contacts
1312
Remove carrier wafer
1314
Probe and test dies
1316
Singulate dies
1318
Sort and Bin dies
1320
Stop

FIG. 13

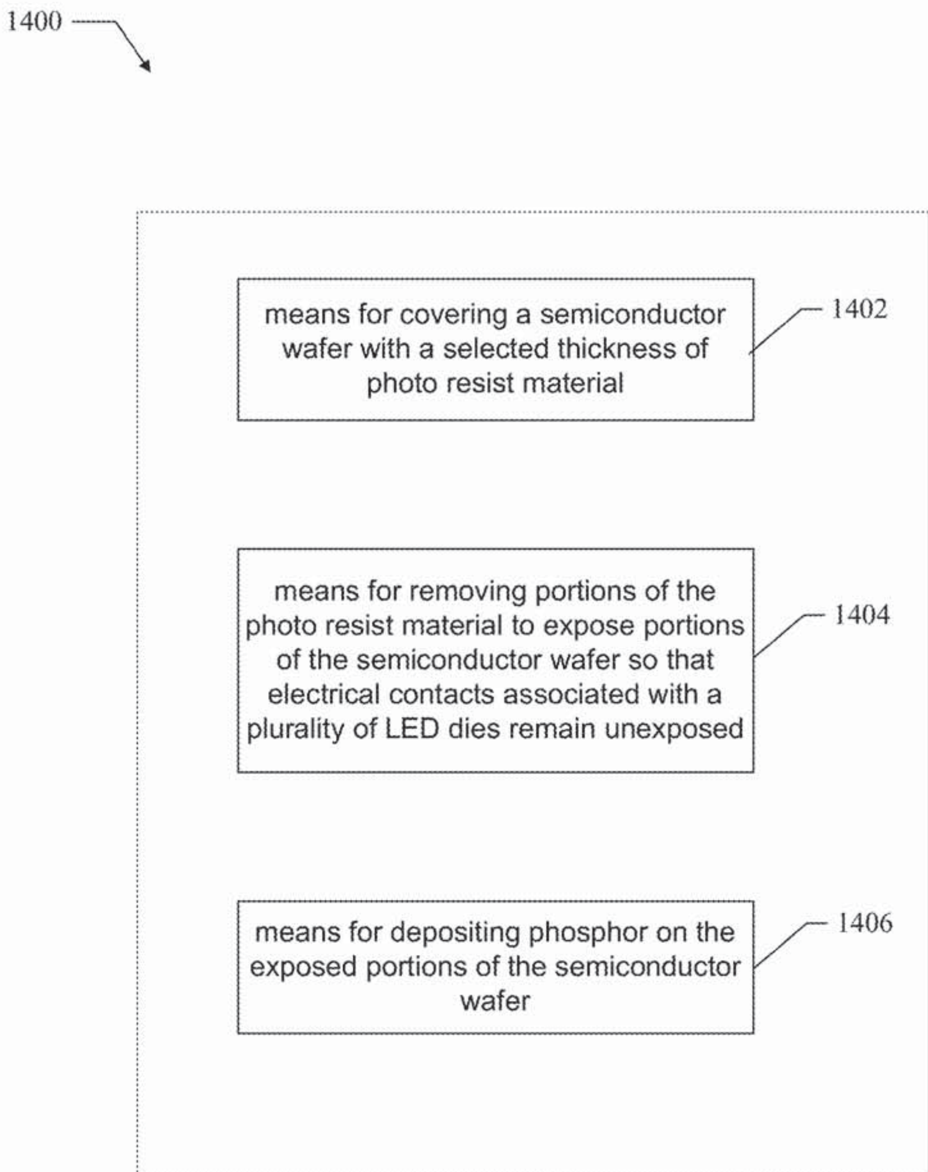

1400
means for covering a semiconductor wafer with a selected thickness of photo resist material
1402
means for removing portions of the photo resist material to expose portions of the semiconductor wafer so that electrical contacts associated with a plurality of LED dies remain unexposed
1404
means for depositing phosphor on the exposed portions of the semiconductor wafer
1406

FIG. 14

SYSTEM FOR WAFER-LEVEL PHOSPHOR DEPOSITION

PRIORITY

This patent application is a continuation application of co-pending U.S. patent application Ser. No. 12/963,011, entitled "System for Wafer-Level Phosphor Deposition," filed on Dec. 8, 2010, in the name of inventor Tao Xu, the disclosure of which is incorporated herein by reference.

RELATED APPLICATION

This application is related to the following co-pending application assigned to the Assignee of the present invention.

a. Application Ser. No. 13/912,024 filed Jun. 6, 2013, entitled "System for Wafer-Level Phosphor Deposition," invented by Tao Xu.

BACKGROUND

Field

The present application relates generally to light emitting diodes, and more particularly, to a system for wafer-level phosphor deposition.

Background

A light emitting diode comprises a semiconductor material impregnated, or doped, with impurities. These impurities add "electrons" and "holes" to the semiconductor, which can move in the material relatively freely. Depending on the kind of impurity, a doped region of the semiconductor can have predominantly electrons or holes, and is referred to as an n-type or p-type semiconductor region, respectively.

In LED applications, an LED semiconductor chip includes an n-type semiconductor region and a p-type semiconductor region. A reverse electric field is created at the junction between the two regions, which causes the electrons and holes to move away from the junction to form an active region. When a forward voltage sufficient to overcome the reverse electric field is applied across the p-n junction, electrons and holes are forced into the active region and combine. When electrons combine with holes, they fall to lower energy levels and release energy in the form of light. The ability of LED semiconductors to emit light has allowed these semiconductors to be used in a variety of lighting devices. For example, LED semiconductors may be used in general lighting devices for interior applications or in various exterior applications.

During manufacture, a large number of LED semiconductor dies are produced on a semiconductor wafer. For example, the wafer may comprise one hundred or more dies. A process referred to as singulation is used to cut the dies from the wafer. The dies may then be coated with a phosphor coating that controls the color of the light emitted from the die when energized. After coating, the dies are probed and tested for color, light intensity output, power consumption and any other types of operational characteristics.

Unfortunately, coating and testing the dies after singulation may be expensive or complicated and make it difficult to obtain dies having consistent color, light intensity output, or other characteristics.

Accordingly, what is needed is a simple and efficient way to apply a phosphor coating on a semiconductor wafer and perform testing prior to singulation to achieve consistent die characteristics and to avoid the expensive and complicated process of working with individual dies.

SUMMARY

In one or more aspects, a system for wafer-level phosphor deposition is provided to allow phosphor coating and testing to be performed on a semiconductor wafer prior to singulation. Thus, the system simplifies the phosphor deposition process and results in individual LED semiconductor dies having consistent operational parameters.

In an aspect, a method is provided for phosphor deposition on a semiconductor wafer comprising a plurality of LED dies. The method comprises covering the semiconductor wafer with a selected thickness of photo resist material, removing portions of the photo resist material to expose portions of the semiconductor wafer so that electrical contacts associated with the plurality of LED dies remain unexposed, and depositing phosphor on the exposed portions of the semiconductor wafer.

In an aspect, an apparatus is provided for phosphor deposition on a semiconductor wafer comprising a plurality of LED dies. The apparatus comprises means for covering the semiconductor wafer with a selected thickness of photo resist material, means for removing portions of the photo resist material to expose portions of the semiconductor wafer so that electrical contacts associated with the plurality of LED dies remain unexposed, and means for depositing phosphor on the exposed portions of the semiconductor wafer.

In an aspect, an LED die is provided that is prepared by a process comprising the operations of covering a semiconductor wafer comprising the LED die with a selected thickness of photo resist material, removing portions of the photo resist material to expose portions of the semiconductor wafer so that electrical contacts of the LED die remain unexposed, depositing phosphor on the exposed portions of the semiconductor wafer, removing remaining photo resist material to expose the electrical contacts of the LED die, and performing a singulation process to cut the LED die from the semiconductor wafer.

Other aspects will become apparent after review of the hereinafter set forth Brief Description of the Drawings, Description, and the Claims.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing aspects described herein will become more readily apparent by reference to the following Description when taken in conjunction with the accompanying drawings wherein:

FIG. **1** shows a side view of an exemplary LED semiconductor wafer obtained from a wafer fabrication process;

FIG. **2** shows a side view of an exemplary wafer assembly comprising the wafer of FIG. **1** attached to a carrier wafer;

FIG. **3** shows the wafer assembly shown in FIG. **2** and further comprising a photo resist layer;

FIG. **4** shows the wafer assembly shown in FIG. **3** after removal of selected portions of the photo resist layer;

FIG. **5** shows a top view of a portion of the wafer assembly shown in FIG. **4**;

FIG. **6** shows the wafer assembly of FIG. **4** after deposition of a phosphor layer;

FIG. **7** shows the wafer assembly of FIG. **6** after removal of photo resist posts;

FIG. **8** shows a top view of a portion of the wafer assembly of FIG. **7**;

FIG. **9** shows the wafer assembly of FIG. **7** after removal of a carrier wafer;

FIG. **10** shows a singulation process performed on the wafer assembly of FIG. **7** to obtain individual LED semiconductor dies;

FIG. **11** shows an exemplary color chart that associates X and Y values with color temperature;

FIG. **12** shows an exemplary color binning graph and table used for sorting and binning LED dies;

FIG. **13** shows an exemplary method for performing wafer-level phosphor deposition; and

FIG. **14** shows an exemplary apparatus for performing wafer-level phosphor deposition.

DESCRIPTION

In various aspects, a system for wafer-level phosphor deposition is provided to allow phosphor coating and testing to be performed on a semiconductor wafer prior to singulation.

The system for wafer-level phosphor deposition is described more fully hereinafter with reference to the accompanying Drawings, in which various embodiments are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the various aspects presented throughout this disclosure. Rather, these aspects are provided so that this disclosure will be complete enough to provide a thorough understanding of the present invention to those skilled in the art. The various aspects of the present invention illustrated in the drawings may not be drawn to scale. Accordingly, the dimensions of the various features may be expanded or reduced for clarity. In addition, some of the drawings may be simplified for clarity. Thus, the drawings may not depict all of the components of a given apparatus (e.g., device) or method.

Various aspects of the present invention will be described herein with reference to drawings that are schematic illustrations of idealized configurations of the present invention. As such, variations from the shapes of the illustrations as a result, for example, manufacturing techniques and/or tolerances, are to be expected. Thus, the various aspects of the present invention presented throughout this disclosure should not be construed as limited to the particular shapes of elements (e.g., regions, layers, sections, substrates, etc.) illustrated and described herein but are to include deviations in shapes that result, for example, from manufacturing. By way of example, an element illustrated or described as a rectangle may have rounded or curved features and/or a gradient concentration at its edges rather than a discrete change from one element to another. Thus, the elements illustrated in the drawings are schematic in nature and their shapes may not be intended to illustrate the precise shape of an element and are not intended to limit the scope of the present invention.

It will be understood that when an element such as a region, layer, section, substrate, or the like, is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present. It will be further understood that when an element is referred to as being "formed" on another element, it can be grown, deposited, etched, attached, connected, coupled, or otherwise prepared or fabricated on the other element or an intervening element.

Furthermore, relative terms, such as "lower" or "bottom" and "upper" or "top," may be used herein to describe one element's relationship to another element as illustrated in the drawings. It will be understood that relative terms are intended to encompass different orientations of an apparatus in addition to the orientation depicted in the Drawings. By way of example, if an apparatus in the Drawings is turned over, elements described as being on the "lower" side of other elements would then be oriented on the "upper" sides of the other elements. The term "lower", can therefore, encompass both an orientation of "lower" and "upper," depending of the particular orientation of the apparatus. Similarly, if an apparatus in the drawing is turned over, elements described as "below" or "beneath" other elements would then be oriented "above" the other elements. The terms "below" or "beneath" can, therefore, encompass both an orientation of above and below.

Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and this disclosure.

As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof. The term "and/or" includes any and all combinations of one or more of the associated listed items

It will be understood that although the terms "first" and "second" may be used herein to describe various regions, layers and/or sections, these regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one region, layer or section from another region, layer or section. Thus, a first region, layer or section discussed below could be termed a second region, layer or section, and similarly, a second region, layer or section may be termed a first region, layer or section without departing from the teachings of the present invention.

FIG. **1** shows a side view of an exemplary LED semiconductor wafer **100** obtained from a wafer fabrication process. For example, in one implementation, the thickness (t) of the LED wafer **100** is approximately 150 micrometers. The wafer **100** comprises any number of LED dies that are exposed on surface **102**. For example, the LED wafer **100** may comprise one hundred or more LED dies having associated electrical contacts and light emitting regions formed on the surface **102**. During operation, the electrical contacts of each die can be energized to cause light to be emitted from the associated light emitting regions.

FIG. **2** shows a side view of an exemplary wafer assembly **200** comprising the LED wafer **100** of FIG. **1** attached to a carrier wafer **202**. For example, in one implementation, the carrier wafer **202** comprises a sapphire carrier wafer that is attached to the LED wafer **100** with thermal release tape **204**. The sapphire carrier wafer **202** operates to support the LED wafer **100** during a phosphor deposition process described below. The thermal release tape allows the sapphire carrier wafer **202** to be easily removed from the LED wafer **100** at a later time. It should be noted that other types of carrier wafers and attachments mechanisms may be used to support the LED wafer **100** during the phosphor deposition process. In one implementation, any suitable automated assembly device is used to assemble the wafer **100** onto the carrier wafer **202** with the thermal release tape **204**.

FIG. **3** shows a side view of a wafer assembly **300** that comprises the wafer assembly **200** and a layer of photo-resist material **302**. The photo-resist material **302** is a light sensitive material that becomes soluble to a photo-resist developer after being exposed to light. Any portion of the photo-resist material **302** that is unexposed to light remains insoluble to the photo-resist developer. In one implementation, the photo-resist material **302** is spin coated to form a thick layer on the LED wafer **100**. For example, the photo-resist material **302** may be approximately two hundred micrometers thick. It should also be noted that any suitable photo resist deposition device may be used to apply the photo-resist material **302** to the wafer assembly **200**.

FIG. **4** shows a side view of a wafer assembly **400** that comprises the wafer assembly **300** after removal of selected portions of the photo-resist layer **302** using a photolithography process. For example, a photolithography device uses light to transfer a geometric pattern from a photo mask onto the light-sensitive photo-resist layer **302**. Light exposed portions of the photo-resist layer **302** are then removed by the photolithography device using a photo-resist developer leaving the unexposed portions remaining. In this example, the unexposed portions are illustrated as photo-resist posts **402**.

In one implementation, the posts **402** are approximately two hundred micrometers tall and are located to cover the p and n electrical contact pads of all the LED dies of the LED wafer **100**. For example, region **404** comprises three photo-resist posts **406**, **408** and **410**. A top view of these posts, as indicated at **412**, is described in greater detail in FIG. **5**.

FIG. **5** shows a top view of the assembly **400** shown in FIG. **4** and provides a detailed illustration of the region **404** from the perspective of the top view indicator **412**. The region **404** comprises the photo-resist posts **406**, **408** and **410** that cover the p and n electrical contacts of the LED dies of the LED wafer **100**. It should be noted that the photo-resist posts **406**, **408**, and **410** may comprise any shape or geometry and are not limited to the shapes shown in FIG. **5**. By covering the p and n contacts, the photo-resist posts protect these contacts from a phosphor deposition layer to be deposited on the surface **502** of the LED wafer **100**. The phosphor deposition operates to control the color of the light emitted by the dies of the LED wafer **100**.

FIG. **6** shows a side view of a wafer assembly **600** that comprises the wafer assembly **300** shown in FIG. **4** after deposition of a phosphor layer **602**. For example, the phosphor deposition may be performed by a deposition apparatus that utilizes any of the following techniques.

1. Electrophoretic Deposition (EPD)
2. Spin Coating
3. Jetting
4. Droplet Deposition
5. Vacuum Evaporation

The phosphor deposition process allows control of the thickness of phosphor layer thereby allowing control of the color of the light emitted from the LED dies. After deposition, the phosphor is allowed to cure. Thus, any suitable phosphor deposition process may be used to apply a phosphor layer having an appropriate thickness onto the wafer assembly **300**. Furthermore, any appropriate phosphor material may be used to achieve a resulting light emission having any desired color.

FIG. **7** shows a side view of a wafer assembly **700** that comprises the wafer assembly **600** shown in FIG. **6** after removal of the photo-resist posts **402**. For example, in one implementation, the photo-resists posts **402** are removed by the photolithography device by exposing the posts to light and applying the appropriate photo-resist developer. Once the photo-resist posts **402** are removed, the phosphor layer comprises regions of phosphor **702** that cover the surface of the LED wafer **100** and cavities **704** that expose the p and n contacts through the phosphor layer. These cavities **704** allow wire bonding of the exposed contacts.

FIG. **8** shows a top view of the assembly **700** shown in FIG. **7** and provides a detailed illustration of the region **404** from the perspective of the top view indicator **412**. The top view shown in FIG. **8** provides a detailed illustration of the region **404** after removal of the photo-resist posts **406**, **408** and **410**. Once the photo-resists posts are removed the p and n contacts underneath the posts are exposed. For example, removal of the posts **406**, **408** and **410** exposes the contacts **802**, **804** and **806**, respectively. Also shown is the semiconductor surface which is now covered by the phosphor deposition **808**.

FIG. **9** shows a wafer assembly **900** that comprises the wafer assembly **700** of FIG. **7** after removal of the carrier wafer. For example, the thermal release tape **204** is heated to release the sapphire carrier wafer **202** so that the LED wafer **100** with phosphor deposition **702** remains.

FIG. **10** shows a singulation process performed on the wafer assembly **900**. The singulation process operates to divide the LED wafer assembly **900** into individual dies. In one implementation, singulation is performed using a front-side laser scribing and breaking device that divides the LED wafer assembly **900** into individual dies (i.e., **1002**, **1004**, and **1006**).

FIG. **11** shows an exemplary color chart **1100** that associates two parameters (X and Y) with color temperature. For example, the color chart **1100** provides X values along the horizontal axis and Y values along the vertical axis. Thus, as indicated by the dashed lines, an X value of 0.32 and a Y value of 0.33 correspond to a color temperature of approximately 6000 Kelvin (K). The color chart **1100** provides a mechanism by which the X and Y values can be used to accurately identify particular colors for the purpose of binning and sorting dies.

In one implementation, the wafer **900** shown in FIG. **9** is probed and tested by a computerized probing device for the purpose of associating X and Y values with each die. Probing the entire wafer at the same time is more efficient than probing individual dies after singulation. During the probing process, each die is energized and various die characteristics are determined. For example, the probing device includes contacts points that are positioned to touch the electrical contacts of each die of the wafer **900**. The electrical contacts are exposed and accessible through the cavities **704** in the phosphor deposition. Once the dies are energized, the probing device measures color temperature, lumen output, voltage, current, and any other operating parameters associated with each die. In an aspect, the measured parameters for each die are mapped to X and Y values based on the color chart **1100**. Thus, each die is associated with it own X and Y values prior to singulation.

FIG. **12** shows a graph **1200** and associated binning table **1202** that can be used to sort and bin LED dies prior to singulation. For example, the graph **1200** defines a number of bins which each include a range of X and Y values from the color chart **1100** of FIG. **11**. In this example, the bin D4 includes the X value of 0.32 and the Y value of 0.33.

Referring now to the binning table **1202**, a numerical arrangement is shown. For example, the bin D**4**, shown at

1204, is associated with a range of X and Y values that include 0.32 and 0.33, respectively. The ANSI color temperature of this range is also shown.

Thus, as each die is separate from the wafer during the singulation process, its associated X and Y value can be used to sort it into the appropriate bin using the binning table **1202**. The dies in each bin can then be place on a tape or packaged using any other packaging method, so that the resulting group of dies will have excellent color consistency. For example, in one implementation, the dies are binned and sorted by a computerized binning device that knows the X and Y values associated with each die.

FIG. **13** shows a method for performing wafer-level phosphor deposition in accordance with the present invention. For example, the method **1300** can be used to perform phosphor deposition as described above with respect to the wafer **100**.

At block **1302**, a LED wafer is obtained from a fabrication process. For example, the wafer **100** is obtained for the wafer-level phosphor deposition process. In one implementation, the wafer **100** comprises one hundred or more LED dies.

At block **1304**, a support carrier is attached to the LED wafer. For example, the sapphire support carrier **202** is attached to the LED wafer using thermal release tape **204**. The support carrier operates to support the LED wafer during the wafer-level phosphor deposition process. In an implementation, any suitable automated assembly device is used to assemble the wafer **100** onto the carrier wafer **202** with the thermal release tape **204**.

At block **1306**, a photo-resist layer is applied to the LED wafer. In one implementation, the photo-resist layer is applied using a spin coating process. For example, the photo-resist layer is applied to the LED wafer **100** and is approximately two hundred micrometers thick. In an implementation, any suitable photo resist deposition device may be used to apply the photo-resist material **302** to the wafer assembly **200**.

At block **1308**, portions of the photo-resist layer are removed so that photo resist posts cover p and n contacts of the LED wafer. For example, as illustrated in FIG. **4**, a photolithography device uses light to transfer a geometric pattern from a photo mask to the light-sensitive photo-resist layer. Light exposed portions of the photo-resist layer are then removed using a photo-resist developer leaving the unexposed portions remaining. The unexposed portions remain as photo-resist posts **402**. FIG. **5** shows a top view that illustrates how the photo-resist posts cover the p and n contacts of the LED wafer.

At block **1310**, phosphor is deposited on the surface of the LED wafer. As illustrated in FIG. **6**, phosphor is disposed on the surface of the LED wafer and surrounds the photo resist posts **402**. For example, a deposition apparatus applies the phosphor to the surface of the LED wafer using at least one of a spin coating, EPD, and jetting process.

At block **1312**, the photo-resist posts are removed exposing the p and n contacts. For example, in one implementation, the photo-resists posts **402** are removed by exposing them to light and applying the appropriate photo-resist developer. Once the photo-resist posts **402** are removed, the phosphor layer comprises regions of phosphor **702** that cover the surface of the LED wafer **100** and cavities **704** that expose the p and n contacts through the phosphor layer.

At block **1314**, the carrier wafer is removed. For example, the thermal release tape is heated to release the sapphire carrier wafer. In an implementation, any suitable automated assembly device is used to disassemble the wafer **100** from the carrier wafer **202**.

At block **1316**, the wafer is probed and tested to determine color temperature, lumen output, power consumption and any other LED characteristics. In addition, the measured color temperature of each die is associated with X and Y values according to the color chart **1100**. In an implementation, the wafer is probed and tested by a computerized probing device.

At block **1318**, a singulation process is performed to divide or cut the LED wafer into individual dies. In one implementation, singulation is performed using a front-side laser scribing and breaking process to divide the LED wafer **900** into individual dies. In one implementation, singulation is performed using a front-side laser scribing and breaking device that divides the LED wafer assembly **900** into individual dies.

At block **1320**, the dies are sorted and binned. For example, the X and Y values determined during the probing and testing process at block **1316** are used to bin the dies according to the bin plot **1200** and the bin table **1202**. For example, the bin plot **1200** defines one or more bins associated with X and Y values. The bins are further defined in the bin table **1202**. The X and Y value of each die is cross-referenced in the bin table **1202** to determine the bin number in which the die is to be grouped. For example, in one implementation, the dies are binned and sorted by a computerized binning device that knows the X and Y values associated with each die.

Therefore, the method **1300** operates to perform wafer-level phosphor deposition in accordance with the present invention. It should be noted that the method **1300** is just one implementation and that the operations of the method **1300** may be rearranged or otherwise modified within the scope of the various aspects. Thus, other implementations are possible with the scope of the various aspects described.

FIG. **14** shows an exemplary apparatus **1400** for performing wafer-level phosphor deposition. For example, the apparatus **1400** is suitable for use to produce the semiconductor wafer **600** shown in FIG. **6**. In an aspect, the apparatus **1400** is implemented by one or more modules configured to provide the functions as described herein. For example, in an aspect, each module comprises hardware and/or hardware executing software.

The apparatus **1400** comprises a first module comprising means (**1402**) for covering a semiconductor wafer with a selected thickness of photo resist material, which in an aspect comprises a photo resist deposition device.

The apparatus **1400** also comprises a second module comprising means (**1404**) for means for removing portions of the photo resist material to expose portions of the semiconductor wafer so that electrical contacts associated with the plurality of LED dies remain unexposed, which in an aspect comprises a photolithography device.

The apparatus **1400** comprises a third module comprising means (**1406**) for means for depositing phosphor on the exposed portions of the semiconductor wafer, which in as aspect comprises a phosphor deposition apparatus.

The description of the disclosed aspects is provided to enable any person skilled in the art to make or use the present invention. Various modifications to these aspects may be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other aspects, without departing from the spirit or scope of the invention. Thus, the present invention is not intended to be limited to the aspects shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein. The word "exemplary" is used exclusively herein to mean "serving as an example, instance, or illustration." Any aspect described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other aspects.

Accordingly, while aspects of a system for wafer-level phosphor deposition have been illustrated and described herein, it will be appreciated that various changes can be made to the aspects without departing from their spirit or essential characteristics. Therefore, the disclosures and descriptions herein are intended to be illustrative, but not limiting, of the scope of the invention, which is set forth in the following claims.

What is claimed is:

1. A method of processing light emitting diode ("LED") apparatus, comprising:

covering a semiconductor wafer containing a plurality of LED dies with a selected thickness of photo resist material;

removing portions of the photo resist material to form a plurality of photo resist posts with bottom surfaces of the plurality of photo resist posts substantially aligned in a first plane and having substantially same height covering electrical contacts associated to the plurality of LED dies from exposure, wherein no photo resist post has a bottom surface in a plane different than the first plane;

depositing a phosphor layer on exposed portions of the semiconductor wafer with a height lower than a height of photo resist posts;

removing remaining photo resist material after depositing the phosphor layer to expose the electrical contacts; and

performing a singulation process.

2. The method of claim **1**, wherein performing a singulation process further includes separating the plurality of LED dies from the semiconductor wafer to form individual dies.

3. The method of claim **1**, further comprising probing the electrical contacts on the semiconductor wafer to determine a plurality of color temperatures associated with the plurality of LED dies.

4. The method of claim **3**, further comprising mapping the plurality of color temperatures to X and Y values associated with a color chart.

5. The method of claim **4**, further comprising performing a singulation process to cut the plurality of LED dies from the semiconductor wafer to form individual dies each having an identified X and Y value.

6. The method of claim **5**, further comprising identifying one or more bins in a binning table, wherein each bin comprises a range of X and Y values.

7. The method of claim **5**, further comprising sorting the individual dies based on their associated X and Y values according to the binning table.

8. The method of claim **1**, further comprising attaching a carrier wafer to support the semiconductor wafer.

9. The method of claim **1**, further comprising growing the plurality of LED dies in the semiconductor wafer.

10. A method of generating a lighting apparatus containing light emitting diode ("LED") dies comprising:

covering a semiconductor wafer including the LED dies with a selected thickness of photo resist material;

removing portions of the photo resist material to form a plurality of photo resist posts and allowing bottom surfaces of photo resist posts to be substantially aligned to a first plane covering at least a portion of electrical contacts associated with the LED dies from exposure, wherein no photo resist post has a bottom surface in a plane different than the first plane;

depositing a phosphor layer on exposed portions of the semiconductor wafer and allowing top surface of the phosphor layer situated below top surfaces of the photo resist posts; and

removing the plurality of photo resist posts to expose electrical contacts of the LED die.

11. The method of claim **10**, further comprising performing a singulation process to cut the LED die from the semiconductor wafer.

12. The method of claim **10**, further comprising probing the electrical contacts on the semiconductor wafer to determine a plurality of color temperatures associated with the LED dies.

13. The method of claim **10**, further comprising performing a singulation process to separate the LED dies from the semiconductor wafer to form individual dies each having an identified X and Y value.

14. The method of claim **13**, further comprising:

identifying one or more bins in a binning table, wherein each bin comprises a range of X and Y values; and

sorting the individual dies based on their associated X and Y values according to the binning table.

15. The method of claim **10**, further comprising growing the plurality of LED dies in the semiconductor wafer.

16. A method of processing a lighting apparatus, comprising:

providing a package configured to house at least one light emitting diode ("LED") die; and

packaging an array of LED dies into the package, wherein the LED dies are fabricated by a method, the method including:

depositing a semiconductor wafer having a plurality of LED dies;

depositing a photo resist material layer over the semiconductor wafer;

removing portions of the photo resist material layer and forming a plurality of posts with bottom surfaces of the plurality of photo resist posts substantially aligned in a first plane and having substantially same post heights covering contacts associated with the plurality of LED dies, wherein no photo resist post has a bottom surface in a plane different than the first plane; and

depositing a phosphor layer with a second height over the semiconductor wafer and allowing the second height of phosphor layer to be lower than the post height.

17. The method of claim **16**, further includes,

removing the plurality of posts to expose the electrical contacts associated to the plurality of LED dies; and

performing a singulation process to cut the LED dies from the semiconductor wafer to form individual dies.

18. The method of claim **16**, further includes probing the electrical contacts to determine a plurality of color temperatures associated with the LED dies.

19. The method of claim **18**, further includes, mapping the plurality of color temperatures to X and Y values associated with a color chart;

performing a singulation process to cut the plurality of LED dies from the semiconductor wafer to form individual dies each having an associated X and Y value;

identifying one or more bins in a binning table, wherein each bin includes a range of X and Y values; and sorting the individual dies based on their associated X and Y values according to the binning table.

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