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(54) **LIGHT EMITTING DIODE PACKAGE HAVING SERIES CONNECTED LEDS**

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(60) Provisional application No. 62/057,189, filed on Sep. 29, 2014.

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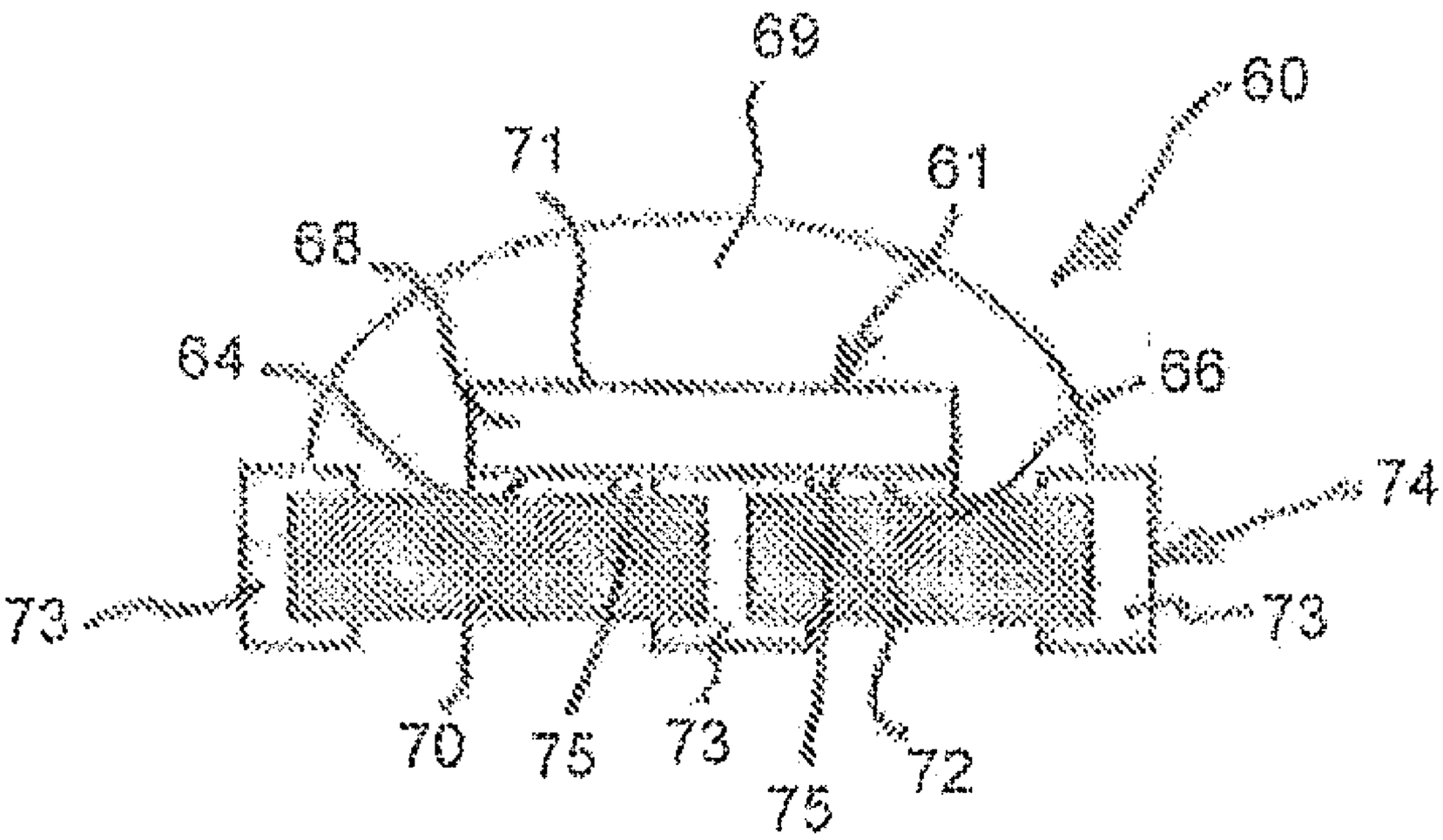
CPC ***H01L 33/62*** (2013.01); ***H01L 25/0753*** (2013.01); *H01L 33/502* (2013.01); *H01L 2924/181* (2013.01); *H01L 2224/48137* (2013.01)

(57) **ABSTRACT**

Light emitting diode packages as disclosed herein include a monolithic chip including at least a first and a second light emitting diode (LED) that are electrically coupled in series, wherein the first and the second LEDs each include at least one electrical terminal configured to be electrically coupled to a power source. The monolithic chip is mounted onto a connection substrate having first and second landing pads formed from metallic material and electrically isolated from each other. The monolithic chip is mounted to the connection substrate such that the electrical terminal of the first LED is electrically connected to the first landing pad and the electrical terminal of the second LED is electrically connected to the second landing pad. In an example, the monolithic chip includes a third and a fourth LED electrically coupled to each other in series, and electrically coupled to the first and second LEDs in parallel.



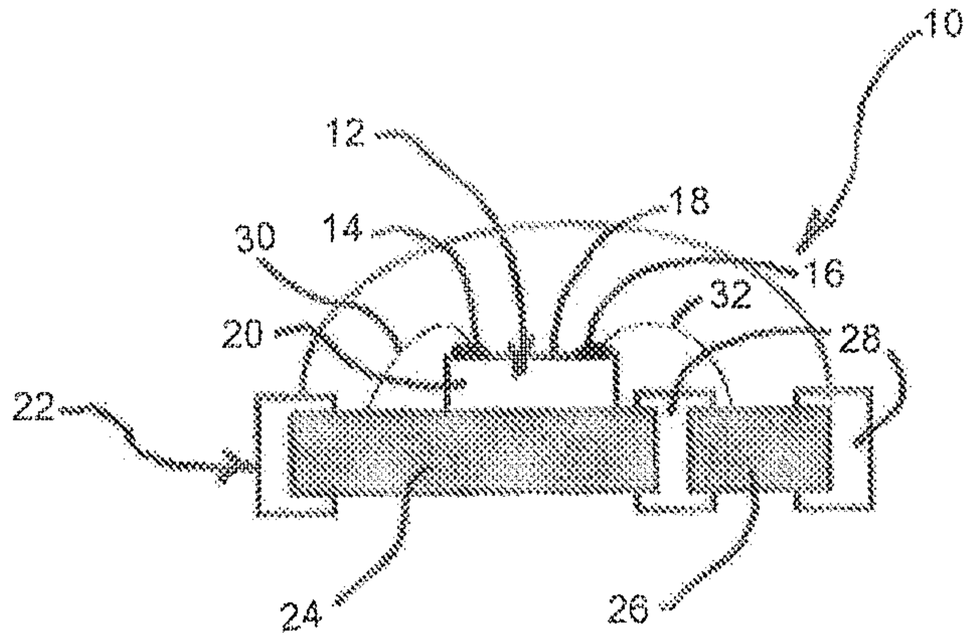


FIG. 1
PRIOR ART

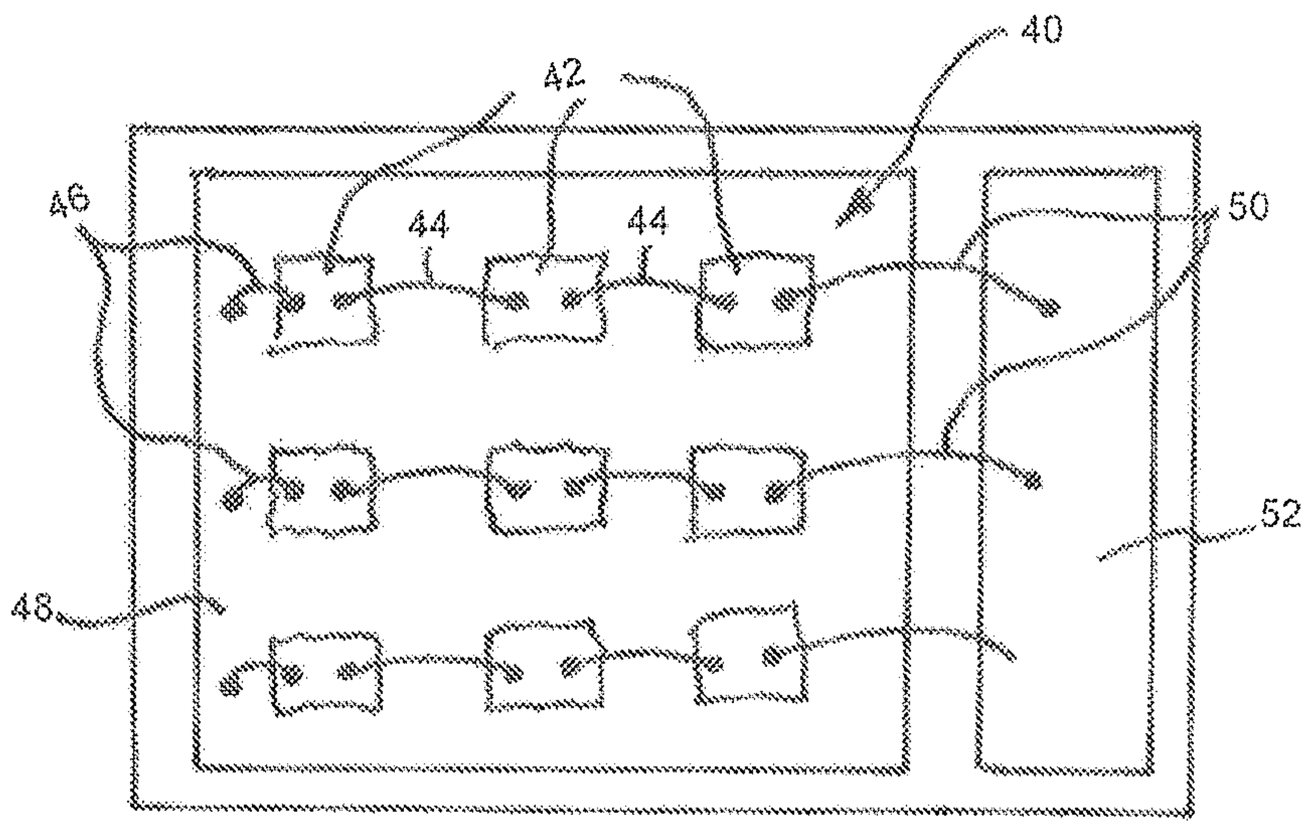


FIG. 2
PRIOR ART

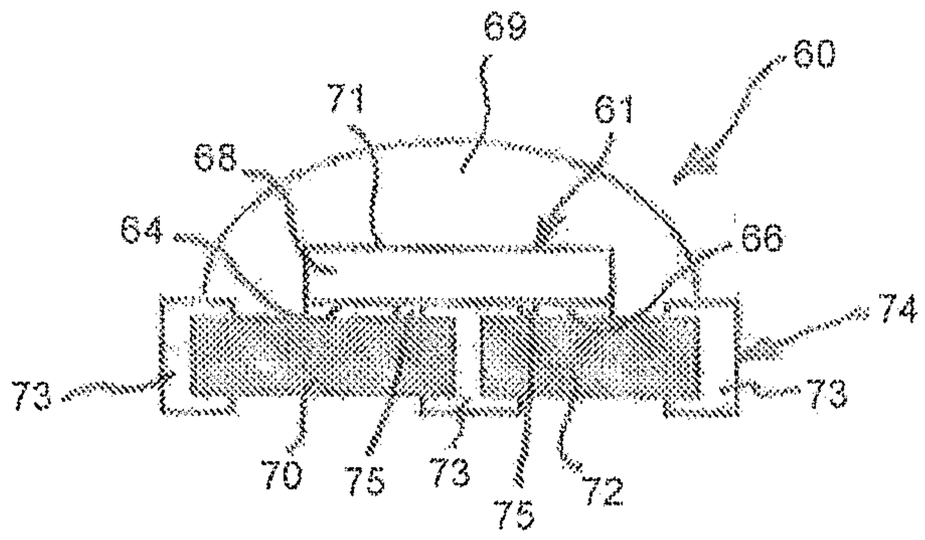


FIG. 3

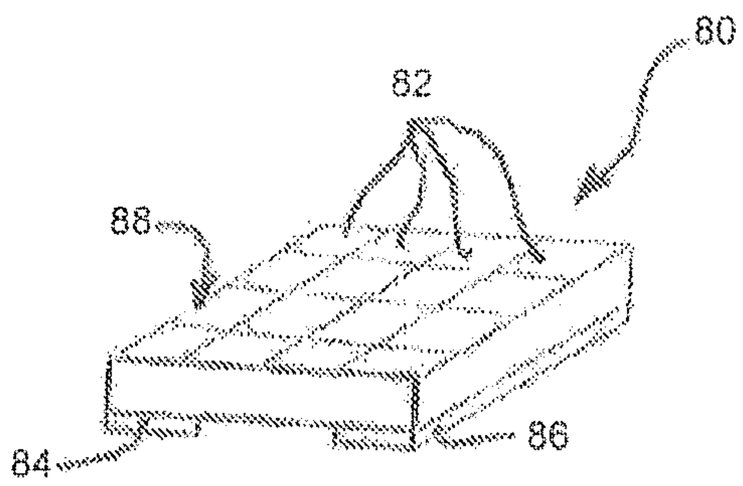


FIG. 4

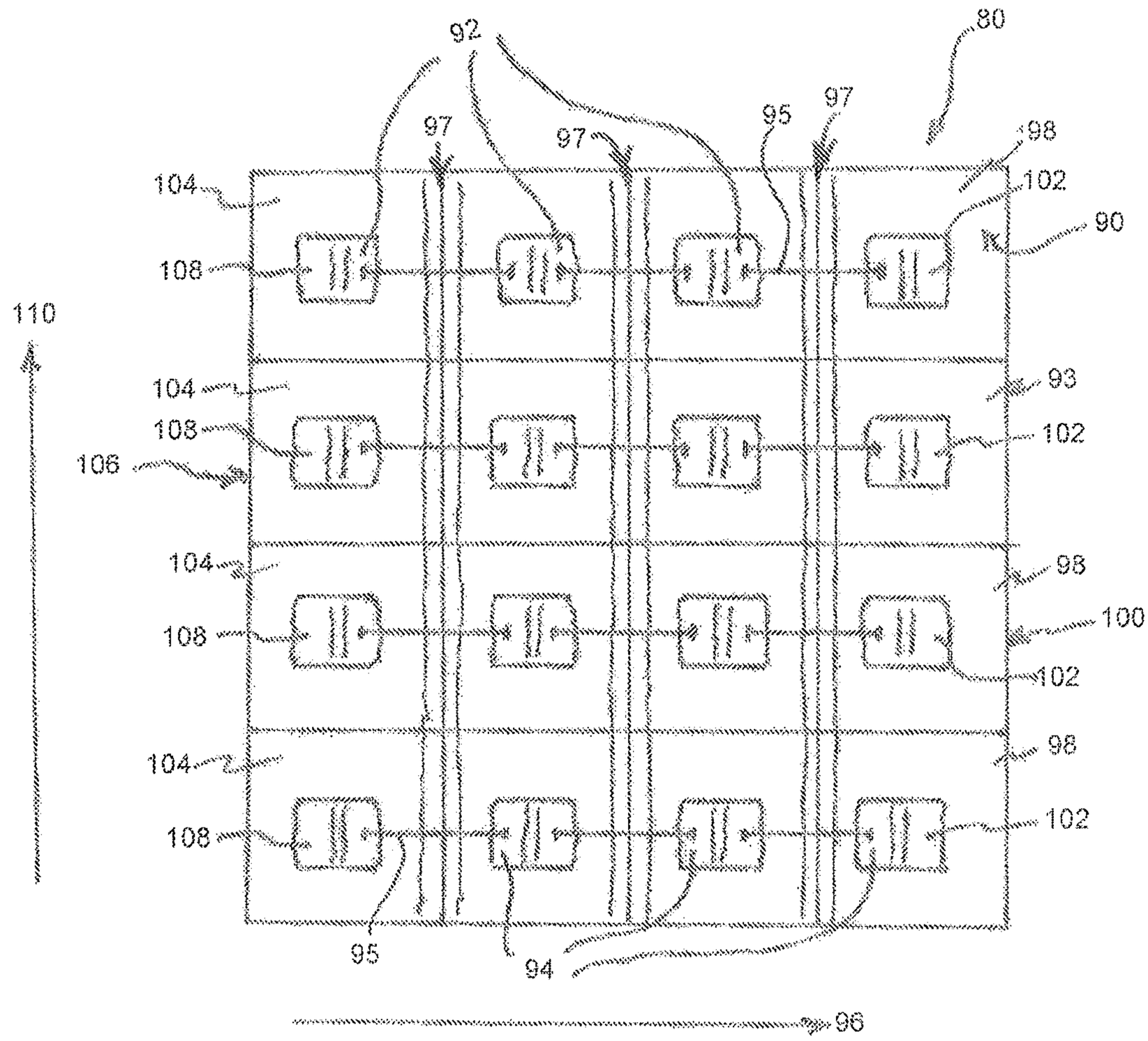

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FIG. 5

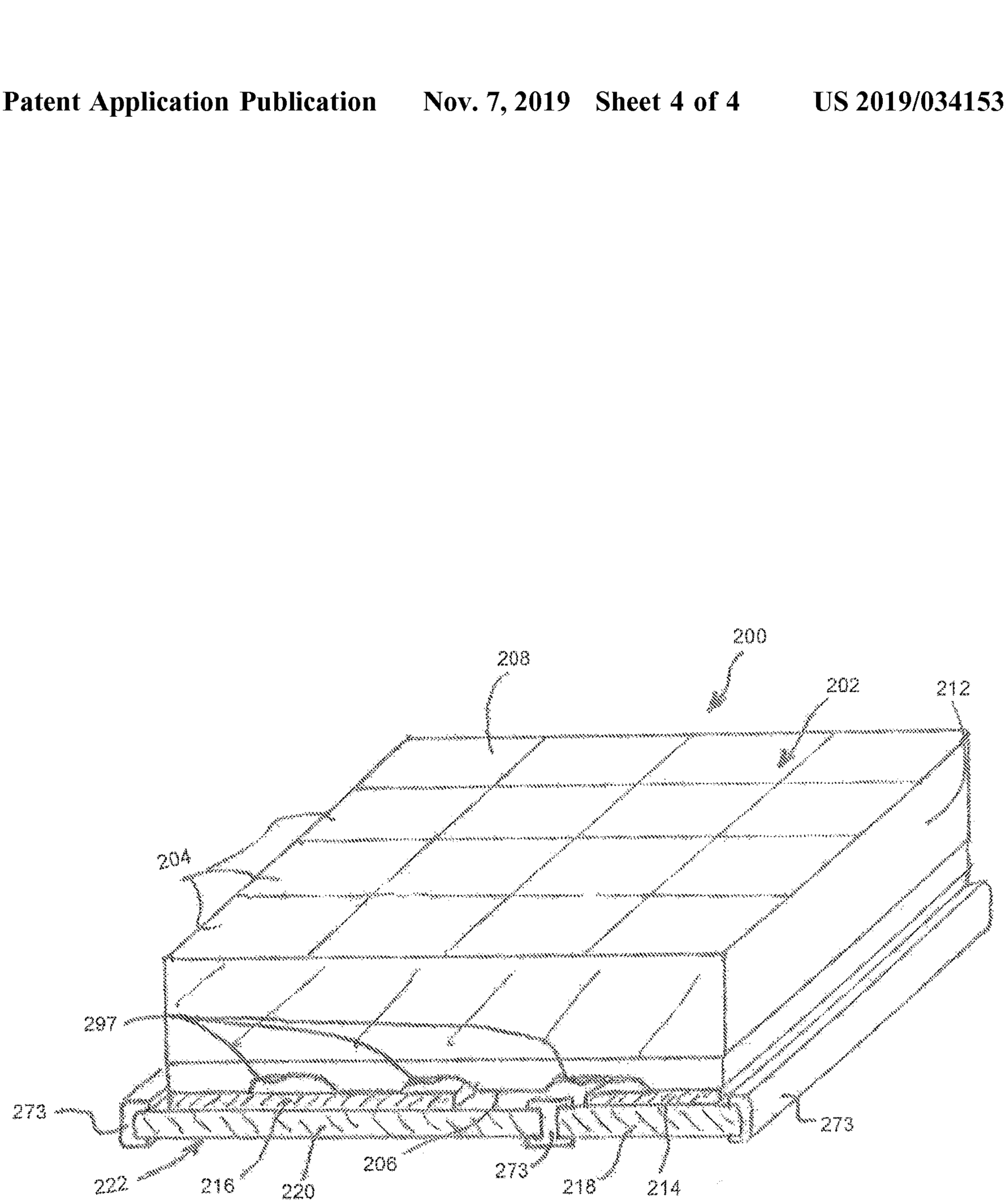

FIG. 6

LIGHT EMITTING DIODE PACKAGE HAVING SERIES CONNECTED LEDS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This patent application is a continuation of U.S. patent application Ser. No. 15/853,413 filed Dec. 22, 2017, which is a divisional of U.S. patent application Ser. No. 14/869,507 filed Sep. 29, 2015, now U.S. Pat. No. 9,853,197 issued Dec. 26, 2017, which claims the benefit of U.S. Provisional Patent Application No. 62/057,189 filed Sep. 29, 2014, which applications are hereby incorporated by reference in their entirety.

FIELD

[0002] Disclosed herein are light emitting diode array constructions, light emitting diode array packages comprising the same, and methods for making the same.

BACKGROUND

[0003] Light emitting diode (LED) packages for end-use lighting applications are known the art. FIG. **1** illustrates an example known LED package **10** comprising a single LED **12**, which is a lateral or vertical LED, comprising a P contact **14** and an N contact **16** positioned along a top surface **18** of the LED and on an LED substrate **20**, e.g., one that active material used to form the P and N junctions is epitaxially grown on. The LED **12** is disposed on a metal substrate **22** comprising P and N electrical terminals **24** and **26** that are separated from one another and held together by an electrically nonconductive material **28**. The LED **12** is electrically connected with the metal substrate by wires **30** and **32** respectively extending from the LED P contact **14** and that is wired bonded to the metal substrate P terminal **24**, and from the LED N contact **16** and that is wire bonded to the metal substrate N terminal **26**. The LED may be encapsulated with a wavelength conversion material **34** to facilitate light emission from the LED in a particular wavelength.

[0004] Arrays of such known LEDs, e.g., two or more lateral or vertical LEDs, may be formed by interconnecting the P contact of one LED to an N contact of an adjacent LED in series by wires extending along the top surface of the LEDs. FIG. **2** illustrates an array **40** of known LEDs, e.g., a 3×3 array of lateral or vertical LEDS, wherein the LEDs **42** in the array are connected with in series to one another by wires **44** extending along the top surface between the P and N contacts of adjacent LEDs. The serially connected LEDs are then connected in parallel to the metal substrate by a wire **46** extending from the P contact of a first LED in the series to the P terminal **48** of the metal substrate, and a wire **50** extending from the N contact of a last LED in the series to the N terminal **52** of the metal substrate.

[0005] A feature of such known LED package is that they are costly to make given the time and labor associated with forming the wired connections from the LED to the metal substrate and, in an array configuration additionally with forming the wired serial electrical connections between the individual LEDs. Further, such LED packages are known to have less than optimal thermal properties, as the LED or LEDs in an array generate a large amount of heat when powered, which heat largely remains in the LED and is not efficiently extracted or removed therefrom during operation, thereby operating to reduce LED service life and reduce the service life of lighting devices or assemblies comprising the same.

[0006] It is, therefore, desired that LED package be constructed in a manner that is both cost efficient to make, and that has improved thermal performance properties when compared to such above-described LED constructions and packages.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] These and other features and advantages of light emitting diode constructions, assemblies comprising the same, and methods for making the same as disclosed herein will be appreciated as the same becomes better understood by reference to the following detailed description when considered in connection with the accompanying drawings.

[0008] FIG. **1** is a cross-sectional side view of a known light emitting diode package;

[0009] FIG. **2** is a top view of a known light emitting diode array package;

[0010] FIG. **3** is a cross-sectional side view of an example monolithic light emitting diode array package as disclosed herein;

[0011] FIG. **4** is a perspective view of an example monolithic light emitting diode array as disclosed herein;

[0012] FIG. **5** is a bottom view of an example monolithic light emitting diode array as disclosed herein; and

[0013] FIG. **6** is a perspective side view of an example monolithic light emitting diode array package as disclosed herein.

SUMMARY

[0014] Light emitting diode packages as disclosed herein comprise a monolithic chip including at least a first and a second light emitting diode (LED) that are electrically coupled in series. The first and the second LEDs each include at least one electrical terminal configured to be electrically coupled to a power source. In an example embodiment, LEDs are flip chip LEDs and the electrical terminals extend along a common surface of the LEDs. The monolithic chip is mounted onto a connection substrate that includes first and second landing pads which are formed from a metallic material and that are electrically isolated from each other. In an example, the connection substrate includes a silicone material interposed between the first and second landing pads and extending around and edge of the connection substrate. The monolithic chip is mounted to the connection substrate such that the electrical terminal of the first LED is electrically connected to the first landing pad and the electrical terminal of the second LED is electrically connected to the second landing pad. In an example, the monolithic chip includes a third and a fourth LED electrically coupled to each other in series, and electrically coupled to the first and second LEDs in parallel. In such example, the first and second terminals operate to provide the parallel electrical connection between the LEDs.

[0015] LED packages as disclosed herein are made by the steps of forming a monolithic wafer comprising a number of LEDs. Forming a series electrical connection between LEDs that are oriented in a sting, and forming a parallel electrical connection between LEDs in the string, wherein the steps of forming the series and parallel electrical connections are done at the wafer level. In an example, the monolithic wafer

may have two or more strings of serially connected LEDs, and the parallel electrical connection between LEDs in the two or more strings may be provided by first and second electrical terminals formed on the monolithic wafer. The so-formed wafer is then connected with the connection substrate so that the first and second electrical terminals are in contact with the connection substrate first and second landing pads to both provide an electrical connection therebetween, and to facilitate the transfer of heat or thermal energy from the monolithic wafer during operation of the LED package to thereby provide improved thermal operating efficiency and performance.

DETAILED DESCRIPTION

[0016] Light emitting diodes (LEDs) and packages comprising the same as disclosed herein are specially constructed having a flip chip architecture configured to promote use in an array and packaging with a metal connection substrate in a manner that is both cost efficient and that provides improved thermal properties when compared to the conventional LED packages discussed above.

[0017] FIG. **3** illustrates an LED package **60** as disclosed herein comprising a monolithic wafer or die **61** comprising one or more LEDs. In an example, the monolithic die may include a single LED and the LED may be a flip chip LED comprising P and N contacts **64** and **66** that are disposed along a common surface of the LED. In such embodiment, the LED comprises a transparent substrate **68** through which light is emitted upon powering the LED, wherein the P and N contacts are positioned along a surface of the LED opposite a top surface **71** of the transparent substrate **68**. The flip chip LED may be formed by conventional technique, e.g., by epitaxially depositing a desired active material onto a compatible substrate material. In an example, the active material may be selected produce light in a blue wavelength in the range of from about 400 to 500 nm, herein referred to as a blue flip chip LED. In an example, the blue flip chip LED comprises an active material formed for example from GaN that has been grown, e.g., epitaxially grown, onto a transparent substrate such as one formed from sapphire or the like having a crystalline lattice structure that is compatible with the active material, e.g., GaN. This is but one example of the type of active material and substrate that can be used to form flip chip LEDs useful for forming LED packages as disclosed herein, and it is to be understood that such example is provided for references and that the types of flip chip LEDs within the scope of the concept as disclosed herein are not limited as to the types of active materials or substrates that may be used to form the same. The LED may be encapsulated with a wavelength converting material **69** such as conformal phosphor or the like for the purpose of converting the wavelength of light produce by the LED to a desired wavelength for an end-use application.

[0018] The LED P and/or N contacts **64** and **66** may be fanned out, or their respective surface area enlarged/expanded, so as to form P and/or N terminals to facilitate connection with respective P and N terminals or contact pads **70** and **72** of a connection substrate **74** used both to accommodate mechanical attachment of the LED and provide electrical power thereto. In an example, the LED P and N contacts or terminals **64** and **66** are sized to both facilitate a desired electrical contact with the respective connection substrate P and N terminals or contact pads **70** and **72**, and to facilitate a desired level of heat or thermal transfer from the LED to the connection substrate to provide an improved level of thermal properties, improving the service life of the LEDs and the package comprising the same. In an example, the P and N terminals **70** and **72** of the connection substrate are formed from a metallic material such as copper or the like.

[0019] As illustrated in FIG. **3**, the P and N terminals **70** and **72** of the connection substrate **74** are separated from one another by an electrically insulating material **73**, which in an example embodiment may be a polymeric material such as silicone or the like. In an example, open spaces **75** may exist between the electrically insulating material **73** and the LED P and N contacts **64** and **66**. An electrically insulating material **73** is also disposed along outer edges of the P and N terminals **70** and **72** and operates both to insulate the outer edges and to hold the P and N terminals together. In an example, the electrically insulating material disposed along the outer edges of the conductive substrate may be formed from the same material used to separate the P and N terminals. In an example, the connection substrate comprising the P and N terminals, the insulating material interposed therebetween, and the insulating material disposed around the edge of the P and N terminals, may be formed by a molding process.

[0020] Example LED packages as disclosed herein may comprise a single LED or a number of LEDs connected with the connection substrate. In an example where the LED package comprises a single LED, such LED comprises a single P contact and single N contact that is placed into contact with the respective P and N terminal of the connection substrate. In an example where the LED package comprises a number of LEDs, such LEDs may be provided in combined form as a monolithic wafer or die, wherein the monolithic wafer comprises a number of P and N contacts associated with each LED, and wherein the P and N contacts are disposed along a common wafer surface.

[0021] FIG. **4** illustrates a monolithic wafer **80** comprising an array of LEDs **82**, and in an example embodiment the LEDs are flip chip LEDs. In the illustrated example, the monolithic wafer comprises a 4×4 array of LEDs or 16 LEDs. However, it is to be understood that the number and arrangement of LEDs in the monolithic wafer may be other than that disclosed and illustrated. For example, the monolithic wafer may comprise two or more LEDs that are oriented extending along a common axis, or may comprise two or more LEDs that are oriented along a first axis and a second axis perpendicular to the first axis, e.g., in an array where the LEDs in the array are in a series-parallel electrical connection. The particular number and arrangement of LEDs within the monolithic wafer is understood to vary depending on the particular end-use application.

[0022] In example illustrated in FIG. **4**, the monolithic wafer **80** comprises P and N terminals **84** and **86** extending along a common surface of the wafer opposite the wafer substrate top surface **88**. The P and N terminals extend in a direction parallel with one another and are in parallel electrical connection with respective P contacts of terminal LEDs positioned at one end of the array, and are in parallel electrical connection with respective N contacts of terminal LEDs positioned at an opposite end of the array. As described above, the P and N terminals **84** and **86** may be configured to provide both a desired degree of electrical contact with the connection substrate, and a desired degree

of thermal transfer from the LED array to the connection substrate to thereby provide improved thermal performance properties during operation.

[0023] FIG. **5** illustrates an underside surface **90** of the monolithic wafer **80** of FIG. **4** prior to forming the P and N terminals (**84** and **86** with reference to FIG. **4**). A feature of LED packages as disclosed herein, comprising the use of a monolithic wafer having a number of LEDs, is the ability to provide a desired series and parallel electrical connection between the LEDs on the wafer itself, i.e., at the wafer level thereby avoiding the costs and labor associated with making such connections by wire bonding among individual LEDs, i.e., after the wafer has been diced to form the separate LEDs. In an example, a series electrical connection is made between the LEDs in each of the rows extending along a common first axis **96** by connecting P contacts **92** of an LED in each row with N contacts **94** of an adjacent LED in the same row. The series electrical connection between the P and N contacts within a row can be made by wire connection **95**, by electrically conductive vias formed in the wafer, or by other electrically conductive element. In an example, the underside surface **90** may comprise recessed regions **97** extending along the wafer between adjacent LEDs in series connection. Again, a feature of the concept as disclosed herein is that such electrical connections between the LEDs are being done at the wafer level.

[0024] The array includes terminal LEDs **98** positioned at one end **100** of each row running along axis **96** that comprises a P contact **102**, and includes terminal LEDs **104** positioned at an opposite end **106** of each row running along axis **96** that comprises an N contact **108**. The LEDs in the rows running along axis **96**, and that are in series electrical connection within the row, are placed into parallel electrical connection with each other by connecting together the P and N contacts **102** and **108** of the end LEDs **98** and **104**, wherein the parallel connection extends along the axis **110**, which is perpendicular to axis **96**. Such parallel electrical connection can be made in the same manner as was done to provide the series electrical connection between the LEDs, e.g., by wire connection, electrically conductive vias formed in the wafer, or by other electrically conductive element, again all taking place at the wafer level. In an example, such parallel connection between the P and N contacts **102** and **108** is made by configuring such respective P and N contacts to connect with one another to form a respective P and N terminal (as illustrated in FIG. **4**), e.g., by fanning out, enlarging or expanding the contact configurations. Alternatively, such parallel connection between the P and N contacts **102** and **108** can be made through the use of separate metallic electrodes that are configured to be attached with each of the respective P and N contacts **102** and **108**, which electrodes thereby form the P and N terminals for the monolithic wafer. The monolithic array and/or the P and N terminals are configured in such a manner so that the P and N terminals do not make direct contact with respective N and P contacts of the LEDs in the array.

[0025] FIG. **6** illustrates an example LED package **200** as disclosed herein comprising monolithic wafer **202** as disclosed above with reference to FIGS. **4** and **5**, comprising a plurality of LEDs **204**, e.g., flip chip LEDs, forming an array that is in series-parallel electrical connection along a common surface **206** opposite a top surface **208** of the wafer, which is a top surface of a transparent substrate **212**. The common surface **206** comprising recessed regions **297** (shown as **97** in FIG. **4**). The monolithic wafer comprises a P terminal **214** and an N terminal **216** that are configured to provide a desired degree of electrical contact with respective P and N terminals or landing pads **218** and **220** of the connection substrate **222** to power the LED array, and to provide a desired degree of heat transfer from the LED array during operation. The connection substrate P and N landing pads **218** and **220** are separated from one another by the electrically insulating material **273**, and the electrically insulating material **273** is also disposed along outer edges of the P and N landing pads **218** and **220** to insulate the outer edges of the LED package.

[0026] A feature of LED packages as disclosed herein is that the LEDs contained therein are provided in the form of a monolithic wafer and the electrical circuitry between the LEDs is formed at the wafer level, thereby reducing production costs. Further, LED packages as disclosed herein comprise flip chip LEDs having P and N terminals disposed along a common surface to facilitate attaching the monolithic LED array to respective P and N terminals or landing pads of a connection substrate wafer. The ability to physically connect the monolithic LED array to the connection substrate through the P and N terminals enables for the thermal transfer of heat from the LED array during operation, thereby providing improved thermal performance properties when compared to the conventional LED packages disclosed above.

[0027] Although certain specific embodiments of LED packages have been described and illustrated for purposes or reference, it is to be understood that the disclosure and illustrations as provided herein not limited to the specific embodiments. Accordingly, various modifications, adaptations, and combinations of various features of the described embodiments can be practiced without departing from the scope what has been disposed herein including the appended claims.

1.-**20**. (canceled)

21. A light emitting diode comprising:

a monolithic chip including:

at a first and a second light emitting diode (LED) that are electrically coupled in series, wherein the first and the second LEDs each include at least one electrical terminal extending along a common surface of the first and second LEDs and configured to be electrically coupled to a power source; and

a third and a fourth LED electrically coupled to each other in series, wherein the third LED is electrically coupled in parallel to the first LED, and wherein the fourth LED is electrically coupled in parallel to the second LED.

22. The light emitting diode as recited in claim **21**, wherein the third and fourth LEDs each include at least one electrical terminal extending along a common surface of the third and fourth LEDs and configured to be electrically coupled to a power source.

23. The light emitting diode as recited in claim **22**, wherein the first and third LEDs share a common first electrical terminal, and wherein the second and fourth LEDs share a common second electrical terminal.

24. The light emitting diode as recited in claim **23**, wherein the first electrical terminal is in electrical contact with all LEDs of the monolithic chip that are in parallel

electrical connection with one another, and wherein the first electrical terminal extends along one underside location of the chip.

25. The light emitting diode as recited in claim **23**, wherein the second electrical terminal is in electrical contact with all LEDs of the monolithic chip that are in parallel electrical connection with one another and extends along one position of the chip, and wherein the second electrical terminal and extends along one underside location of the chip.

26. The light emitting diode as recited in claim **21**, wherein the chip comprises a first electrical terminal and a second electrical terminal disposed along an underside of the chip and separated from one another, wherein the first and second electrical terminals are each connected to respective LEDs that are in parallel electrical connection with one another.

27. The light emitting diode as recited in claim **26** wherein the first and second electrical terminals are positioned on the chip parallel with one another.

28. The light emitting diode as recited in claim **26** wherein the first electrical terminal is located along one edge of the chip and the second electrical terminal is located along a second opposed edge of the chip.

29. The light emitting diode as recited in claim **21** comprising a connection substrate having a first and second landing pad, wherein the electrical terminal of the first LED is in electrical connection with the first landing pad and the electrical terminal of the second LED is in electrical connection with the second landing pad.

30. The light emitting diode as recited in claim **29**, wherein the connection substrate first and second landing pads are electrically isolated from each other.

31. A monolithic wafer comprising an array of flip chip light emitting diodes (LEDs) arranged in a number of rows extending along a first axis of the wafer, wherein the LEDs within each row are in series electrical connection with each other, wherein the LEDs at opposed ends of each row are in parallel electrical connection with one another extending along a second axis of the wafer, wherein array of LEDs is in series-parallel connection, wherein the monolithic wafer comprises first and second electrical terminals that extend along a common surface of the wafer and that are in electrical connection with the LEDs.

32. The monolithic wafer as recited in claim **31**, wherein the first electrical terminal extends along one of the wafer first axis or second axis, and the second electrical terminal extends along the other of the wafer first axis or second axis.

33. The monolithic wafer as recited in claim **31**, wherein the LEDs at the opposed ends of the rows are in electrical connection with the respective first and second electrical terminals.

34. The monolithic wafer as recited in claim **31** comprising a connection substrate in electrical connection with the array of LEDs, wherein the connection substrate is disposed along the common surface wafer comprising the first and second electrical terminals.

35. The monolithic wafer as recited in claim **34**, wherein the connection substrate comprises first and second landing pads that are in electrical connection with the respective first and second electrical terminals.

36. The monolithic wafer as recited in claim **35**, wherein the connection substrate comprises an electrically isolating material interposed between the first and second landing pads.

37. A method for making a light emitting diode (LED) array comprising the steps of:

forming a monolithic wafer comprising a number of LEDs each having P and N contacts;

forming two or more strings of LEDs, wherein the LEDs within each string have P and N contacts that are in series connection with one another; and

forming a parallel connection between the LEDs in the two or more strings by connecting together the P contacts of an LED from each string, and connecting together the N contact of an LED from each string.

38. The method as recited in claim **37** further comprising:

forming a P terminal on the wafer that is in electrical connection with the parallel P contacts of the LEDs; and

forming an N terminal on a surface of the wafer common to the P terminal, wherein the N terminal is in electrical connection with the parallel N contacts of the LEDs.

39. The method as recited in claim **38** further comprising:

forming an electrical connection between the P terminal and a first landing pad of a connection substrate disposed adjacent the wafer surface; and

forming an electrical connection between the N terminal and a second landing pad of the connection substrate.

40. The method as recited in claim **39**, wherein the connection substrate first landing pad and second landing pad are electrically isolated from one another.

* * * * *